MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

A-SERIES TRAINING MANUAL

A-series maintenance course

MITSUBISHI ELECTRIC

REVISIONS

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

MAINTENANCE

CONTENTS

1. PC CPU

1.1 Configuration of a PC CPU

When a PC CPU is considered as a control ladder, it can be expressed as an input ladder, output ladder, and a program as shown below.

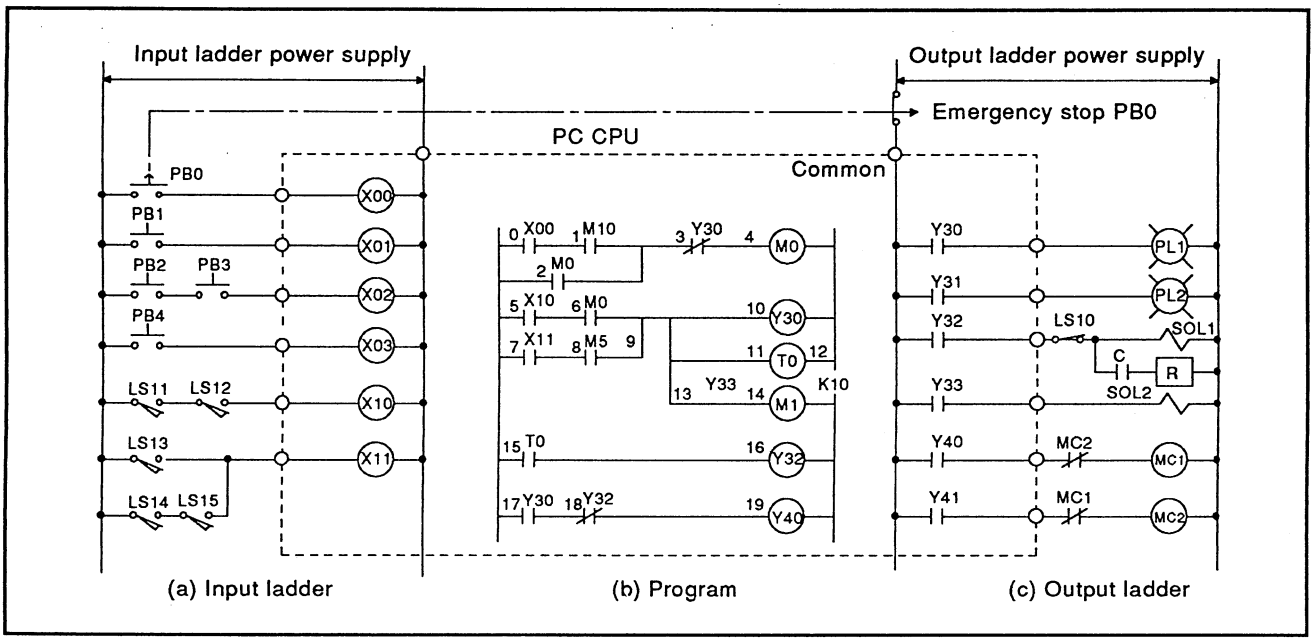


Fig. 1.1 Configuration of a PC CPU

1.2 Devices

This section explains the devices that can be used for a MELSEC-A.
The number of points that can be used varies with the type of CPU module.

1.2.1 Input/output X and Y

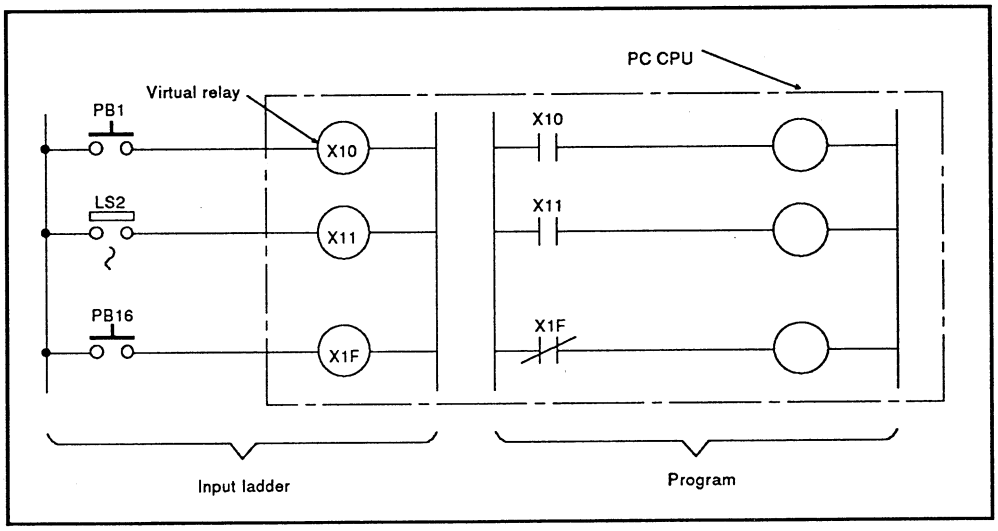
Input/output X and Y are used for communications between a PC CPU and an external device.

(1) Input X

(a) Inputs give commands and data from external devices such as select switches, limit switches, and digital switches to the PC CPU.

(b) As for the 1=point input, virtual relay Xn is incorporated in the PC CPU and the N/O contact and N/C contact of that Xn are used in the program.

(c) There are no restrictions on the number of Xn N/O contracts and N/C contacts that can be used in the program.



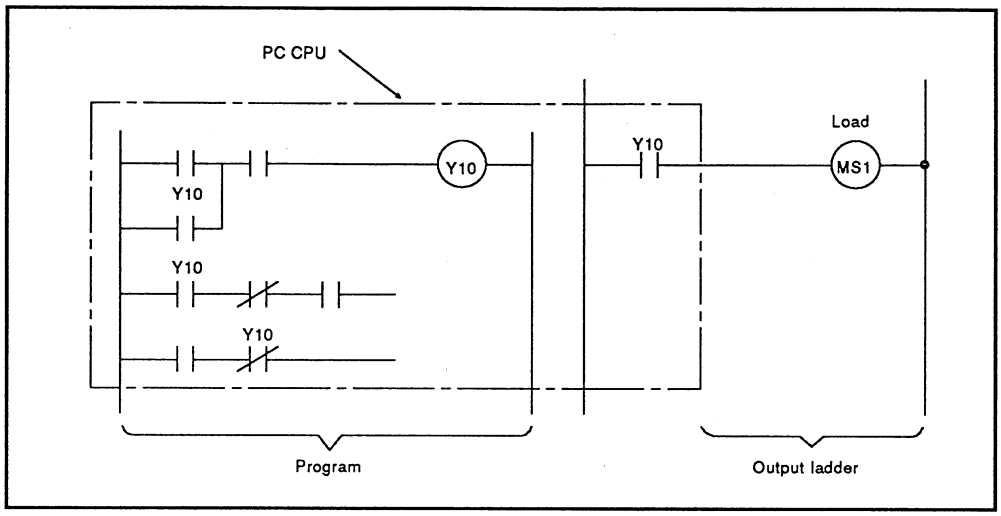
(d) Input X numbers are expressed in hexadecimal (0 to 9 and A to F).

(2) Output Y

(a) Outputs provide program control results to external devices such as solenoids, magnetic switches, signal lamps, and digital indicators.

(b) Outputs can be externally fetched as an equivalent to a single N/O contact.

(c) There are no restrictions on the number of Yn N/O contacts and N/C contacts that can be used in the program.



(d) Output Y numbers are expressed in hexadecimal (0 to 9 and A to F).

(e) An output Y that corresponds to an area loaded with an input unit and an area not loaded with a unit can be used instead of internal relay M.

(f) If Y is used as an internal relay M, it cannot be latched.

(g) As shown below, output Y is controlled by the RUN keyswitch.

RUN Keyswitch	Output States
STOP	Output is turned OFF.
RUN	Operation result is output.
PAUSE	Output in the RUN state is held.
STOP → RUN	After outputting the operation result in the STOP state again, the operation result is output.
PAUSE → RUN	After outputting the output in the PAUSE state again, the operation result is output.

1.2.2 Internal relay M and latch relay L

Internal relay M and latch relay L are internal aux. relays of a PC CPU that cannot be directly output externally.

(1) Internal relay M

(a) Data is cleared by turning ON the power supply or by switching the reset switch on the front of the CPU to RESET.

When the RUN keyswitch is set to STOP, data is cleared by switching the reset switch to LATCH CLEAR.

(b) There are no restrictions on the number of internal relay N/O contacts and N/C contacts that can be used in the program.

(c) Internal relay M numbers are expressed in decimal (0 to 9).

(2) Latch relay L

(a) The former state will be held even if the power supply is turned OFF.

Data is not cleared even when the power supply is turned ON or the reset switch on the front of the CPU is switched to RESET.

(b) There are no restriction on the number of latch relay N/O contacts and N/C contacts that can be used in the program.

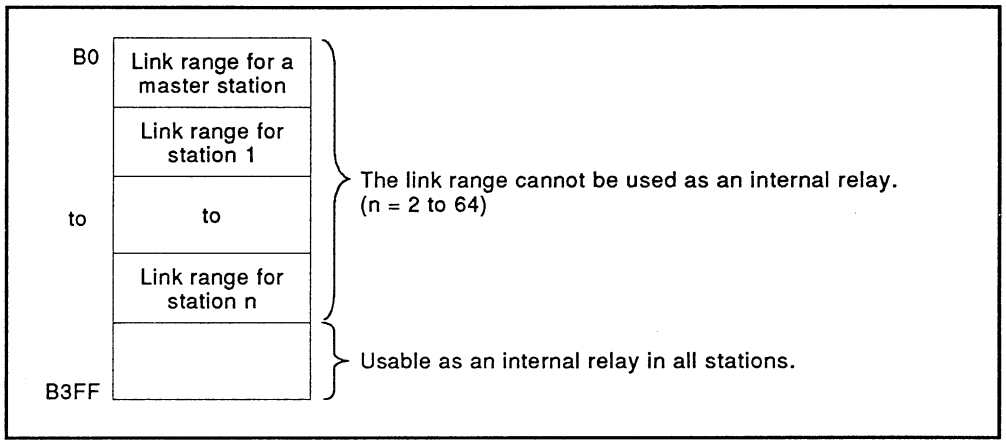
(c) Latch relay L numbers are expressed in decimal (0 to 9).

1.2.3 Link relay B

Link relay B is used for the MELSECNET data link.
Link relay B cannot be externally output as output Y.

(1) Link relay B

(a) The B number to be used by the parameter setting's link parameter setting by utilizing a peripheral device (such as a GPP) is allocated to link relay B. A range that is not set can be used instead of an internal relay.



(b) There are no restriction on the number of link relay N/O contacts and N/C contacts that can be used in the program.

(c) Link relay B numbers are expressed in decimal (0 to 9, and A to F).

1.2.4 Annunciator F

The annunciator is used with the external fault detection program that corresponded to the annunciator F number.
Therefore, when an external fault occurs, the contents of the fault are detected by using an F number.

(1) Annunciator F

(a) When an external fault condition goes ON, the F number is stored in a special data register (D9124 to D9132).
In addition, a special relay (M9009) goes ON.

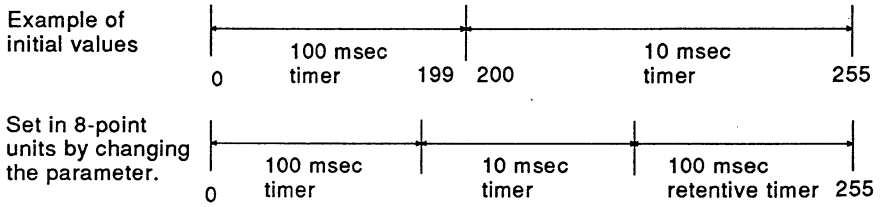
(b) When annunciator F goes ON, the ERROR LED on the front of the CPU flashes.
If the CPU has a LED indicator, it displays the F number.

(c) Annunciator F has a relay function.
N/O and N/C contacts can be used with the program.

(d) Annunciator F numbers are expressed in decimal (0 to 9).

1.2.5 Timer T

The PC CPU uses three kinds of upcount timers: 10 msec timers, 100 msec timers, and 100 msec retentive timers.
As for number allocation, initial values are set.
However, they can be changed in 8-points units.



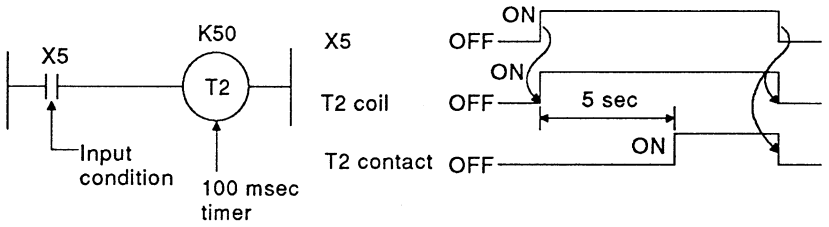
(1) 100 msec timer T

(a) When the input condition has been established, the measurement is started.

And then, when the current value equals the set value, the timer contact goes ON.

(b) If an input condition becomes disestablished, the measurement value of the 100 msec timer becomes 0, and the contact goes OFF.

Example



(c) Set the set value in decimal.

When 5.0 seconds is set, it is K50.
Also, the data in data register D can be set to a set value (0.1 to 3276.7 seconds).

(d) The precision is +2 scan time and -1 scan time.

(The time from when the input condition goes ON until the timer contact operates)

(e) Timer T numbers are expressed in decimal (0 to 9).

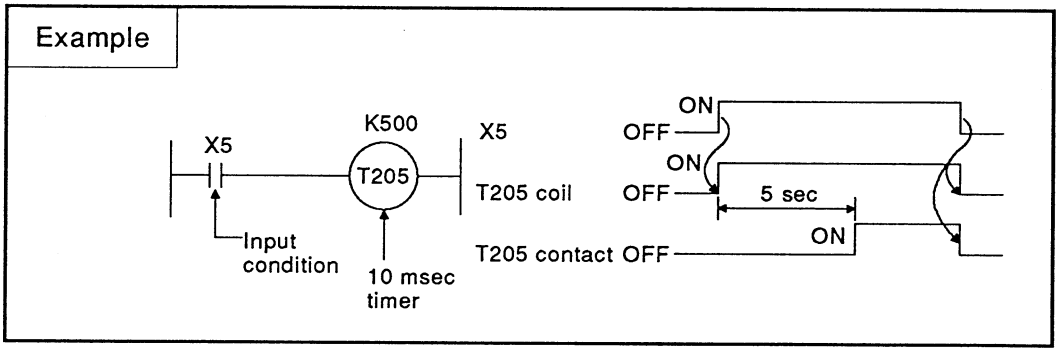
(2) 10 msec timer T

(a) When the input condition has been established, the measurement is started.

And then, when the current value equals the set value, the timer contact goes ON.

(b) If an input condition becomes disestablished, the measurement value of the 10 msec timer becomes 0, and the contact goes OFF.

Example



(c) Set the set value in decimal.

When 5.00 seconds is set, it is K500.
Also, the data in data register D can be set to a set value (0.01 to 327.67 seconds).

(d) The precision is +2 scan time and -1 scan time. (The time from when the input condition goes ON until the timer contact operates)

(e) Timer T numbers are expressed in decimal (0 to 9).

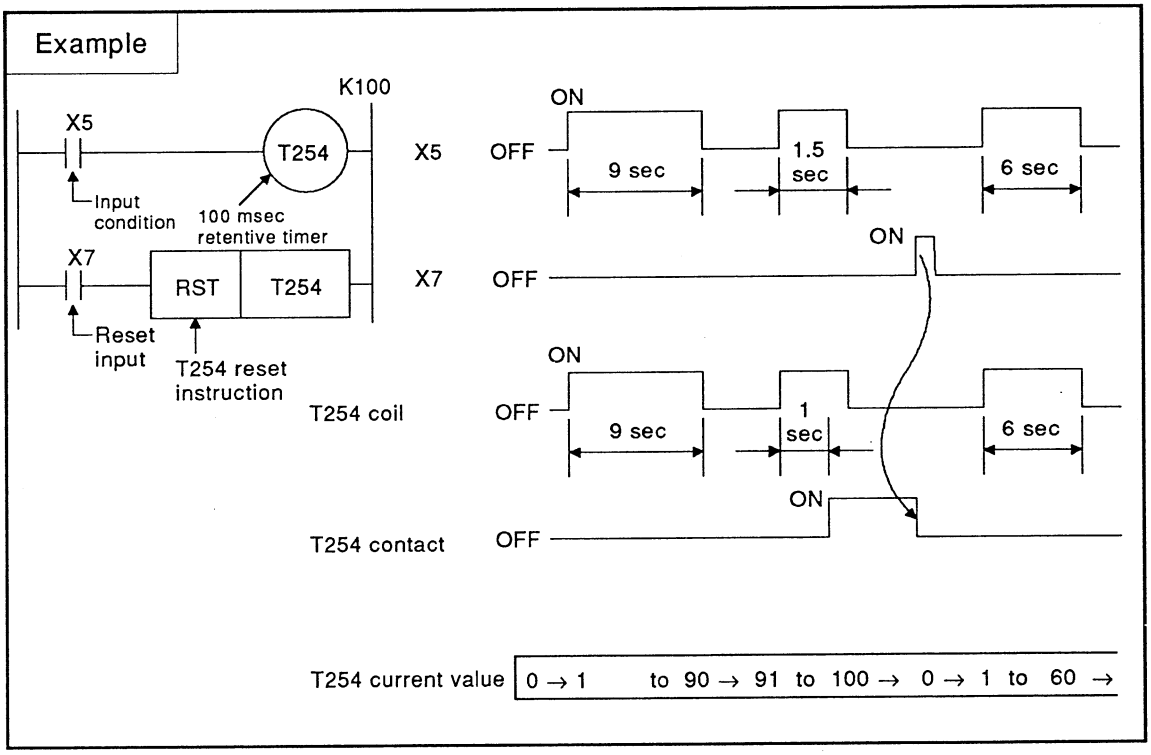
(3) 100 msec retentive timer

(a) When the input condition has been established, the measurement is started.

(b) And then, when the current value equals the set value, the timer contact goes ON.

Even if the input condition becomes disestablished, the current value (measurement value) of the 100 msec retentive timer is held and the contact state does not change.

(c) The measurement value of the 100 msec retentive timer becomes 0 by executing the RST instruction, and then the contact goes OFF.



(d) Set the set value in decimal. When 10.0 seconds is set, it is K100. Also, the data in data register D can be set to a set value (0.1 to 3276.7 seconds).

(e) The precision is ascertained by the following formula:

+2a scan time to -a scan time

a: The number of ON times until count out

(f) Timer T numbers are expressed in decimal (0 to 9).

1.2.6 Counter C

Counter C detects the ON/OFF of an input condition in an addition expression and also counts (adds).

(1) Counter C

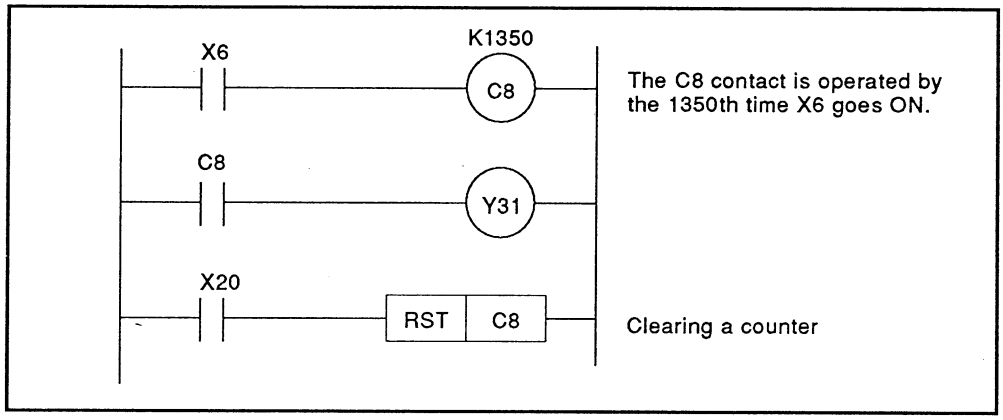
(a) Set the set value in decimal. K1350 is the count that can be added to 1350. Also, data in data register D can be set to a set value. The max. set value is 32767.

(b) The max. count speed is shown below.

Max. count speed (time/sec)
$\frac{10n}{ts}$

ts: Scan time (unit: msec)
n : Duty (%)

(c) Even if the input condition goes OFF, the count value in the counter is not cleared. Use an RST instruction to clear the count value in a counter.



(d) Some CPUs can use a counter as an interruption counter by creating a counter in the interruption program and setting it in the parameter as an interrupt.

(e) Counter numbers are expressed in decimal (0 to 9).

1.2.7 Data register D

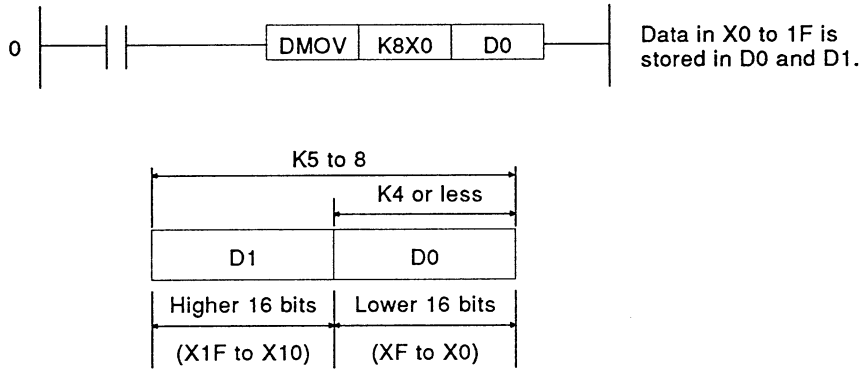
Data register D is the memory where data in the PC CPU is stored.

(1) Data register D

(a) A 1-point data register is composed of 16 bits. Read/write is enabled in 16-bit units.

(b) 2 points are used to handle 32-bit data. The data register number designated by the 32-bit instruction holds 16 bits and the designated data register number + 1 holds the higher 16 bits.

Example When the DMOV instruction is used



(c) Data stored in a sequence program is held until other data is stored.

(d) Data stored in a data register is cleared by turning ON the power supply or switching the reset switch to RESET. Also, when the RUN keyswitch is set to STOP, data is cleared by switching the reset switch to LATCH CLEAR.

(e) Values that can be stored

	Decimal	Hexadecimal
16 bits	-32768 to 32767	0 to FFFF
32 bits	-2147483648 to 2147483647	0 to FFFFFFFF

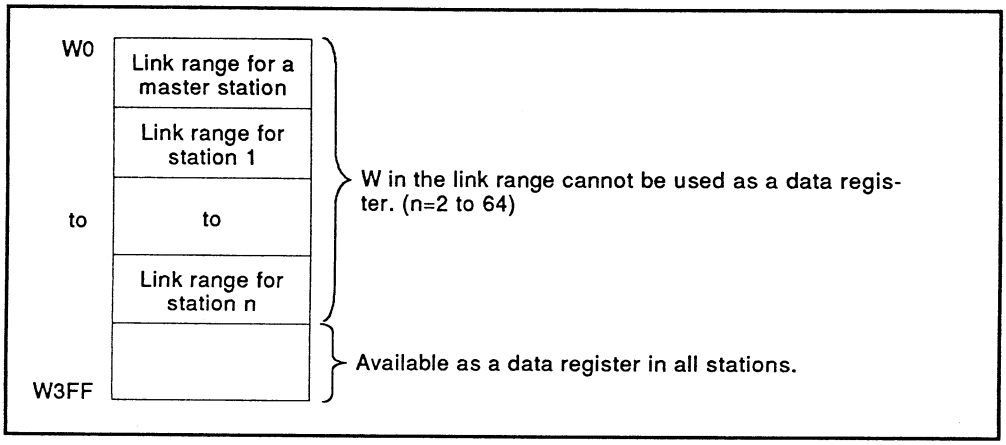
(f) Data register D numbers are expressed in decimal (0 to 9).

1.2.8 Link register W

Link register W is the data register in the MELSECNET data link.

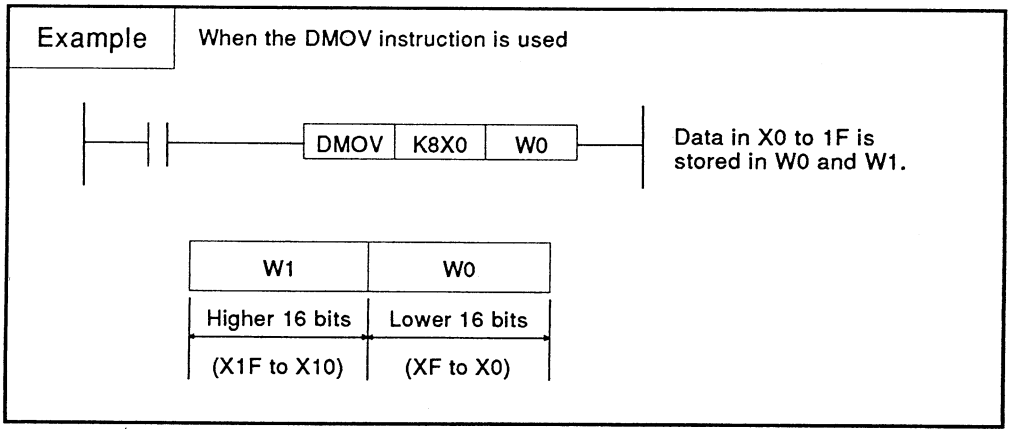
(1) Link register W

(a) The W number to be used by the link parameter setting of the parameter of a peripheral device (such as a GPP) is allocated to the link register. A range that is not set can be used instead of a data register.



(b) A 1-point link register is composed of 16 bits. Read/write is enabled in 16-bit units.

(c) 2 points are used to handle 32-bit data. The link register number designated by the 32-bit instruction holds 16 bits and the designated link register number + 1 holds the higher 16 bits.



(d) Data stored in a link register is cleared by turning ON the power supply or switching the reset switch to RESET. Also, when the RUN keyswitch is set to STOP, data is cleared by switching the reset switch to LATCH CLEAR.

(e) Values that can be stored

	Decimal	Hexadecimal
16 bits	-32768 to 32767	0 to FFFF
32 bits	-2147483648 to 2147483647	0 to FFFFFFFF

(f) Link register W numbers are expressed in hexadecimal (0 to 9, and A to F).

1.2.9 File register R

File register R can be used with data register D in the same way as for a sequence program.

(1) File register R

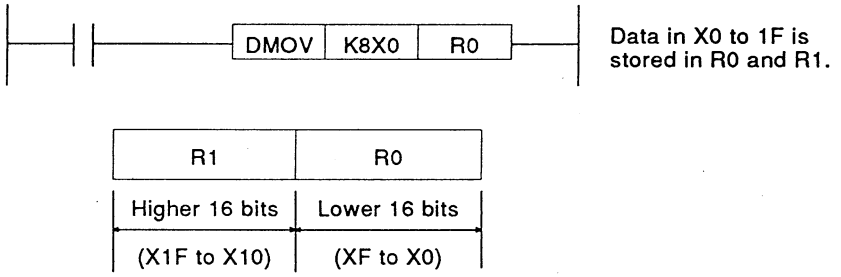
(a) The file register can be used to enlarge the data register. It can be utilized by setting the number of device points by using the parameter's memory capacity setting.

(b) The user memory area is utilized for a file register.

(c) A 1-point file register is composed of 16 bits. Read/write is enabled in 16-bit units.

(d) 2 points are used to handle 32-bit data. The file register number designated by the 32-bit instruction holds 16 bits and the designated file register number + 1 holds the higher 16 bits.

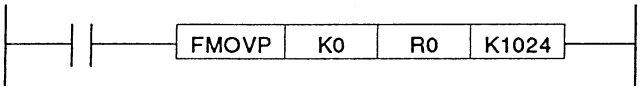
Example When the DMOV instruction is used



(e) Data stored in a file register holds its state even when the power supply is turned OFF. Data is not cleared even if the power supply is turned ON or the reset switch is set to RESET. If the RUN keyswitch is set to STOP, data cannot be cleared by switching the reset switch to LATCH CLEAR.

(f) Write 0 by using an MOV(P) or FMOV(P) instruction to clear the file register.

Example When R0 to 1023 (1 Kpoint) is cleared



(g) Values that can be stored

	Decimal	Hexadecimal
16 bits	-32768 to 32767	0 to FFFF
32 bits	-2147483648 to 2147483647	0 to FFFFFFFF

(h) File register R numbers are expressed in decimal (0 to 9).

1.2.10 Accumulator A

Accumulator A is the data register in which the operation results of the basic instructions and application instructions are stored.

(1) Accumulator A

(a) The operation results of the following basic instructions and application instructions can be stored:

Instructions	Functions	Instructions	Functions	Instructions	Functions
SER	Data search	ROR	Accumulator right rotation	ROL	Accumulator left rotation
SERP		RORP		ROLP	
SUM	Bit check	DROR		RCL	
SUMP		DRORP		RCLP	
DSUM		RCR		DROL	
DSUMP		RCRP		DROLP	
———		DRCR		DRCL	
		DRCRP		DRCLP	

(b) When the above instructions are not used, the accumulator can be used with a sequence program as well as a data register.

(c) A 1-point data register is composed of 16 bits. Read/write is enabled in 16-bit units.

(d) Two accumulators (A0 and A1) are provided. Accumulator A0 holds the lower 16 bits and A1 holds the higher 16 bits when used with a 32-bit instruction. Therefore, A1 cannot be designated when a 32-bit instruction is used.

(e) Data stored in an accumulator is cleared by turning ON the power supply or switching the reset switch to RESET. Also, when the RUN keyswitch is set to STOP, data is cleared by switching the reset switch to LATCH CLEAR.

(f) Values that can be stored

	Decimal	Hexadecimal
16 bits	-32768 to 32767	0 to FFFF
32 bits	-2147483648 to 2147483647	0 to FFFFFFFF

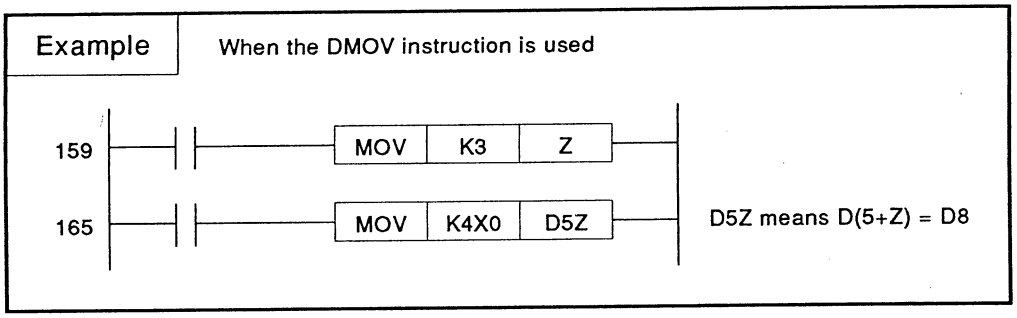
(g) Accumulator A numbers are expressed in decimal (0 to 9).

1.2.11 Index registers Z and V

Index registers Z and V add contents to device (X, Y, M, B, L, F, T, C, D, W, R, K, H, and P) numbers and indirectly change device numbers.
Devices to be allocated vary with the type of CPU module.

(1) Index registers Z and V

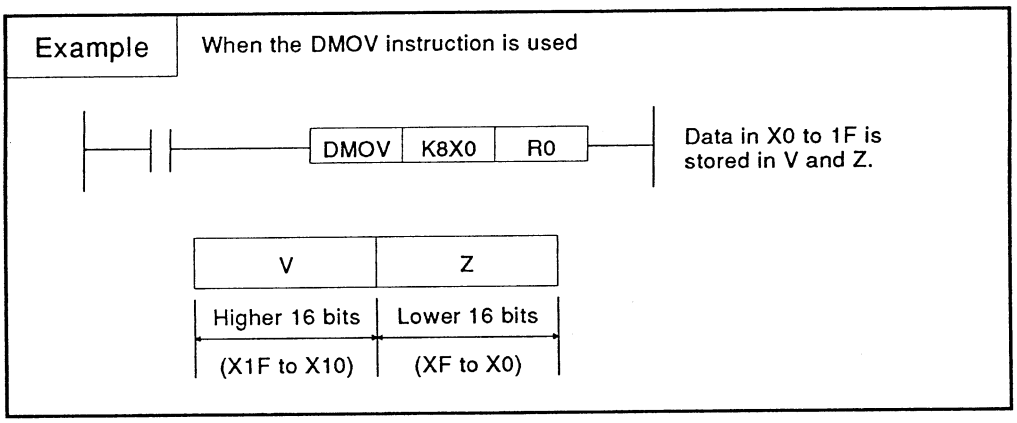
(a) Program example



(b) An index register can be used for a sequence program as well as a data register.

(c) A 1-point index register is composed of 16 bits. Read/write is enabled in 16-bit units.

(d) Index register Z holds the lower 16 bits and V holds the higher 16 bits. Therefore, V cannot be designated when a 32-bit instruction is used.



(e) Data stored in an index register is cleared by turning ON the power supply or switching the reset switch to RESET. Also, when the RUN keyswitch is set to STOP, data is cleared by switching the reset switch to LATCH CLEAR.

(f) Values that can be stored

	Decimal	Hexadecimal
16 bits	-32768 to 32767	0 to FFFF
32 bits	-2147483648 to 2147483647	0 to FFFFFFFF

(g) Index registers Z and V numbers are expressed in decimal (0 to 9).

REMARK

Z1 to Z6 and V1 to V6 can be used only with an A2A and A3ACPU. The following chart shows the combinations for handling them as 32-bit data.

Higher 16 Bits	Lower 16 Bits
V1	Z1
V2	Z2
V3	Z3
V4	Z4
V5	Z5
V6	Z6

1.2.12 Nesting N

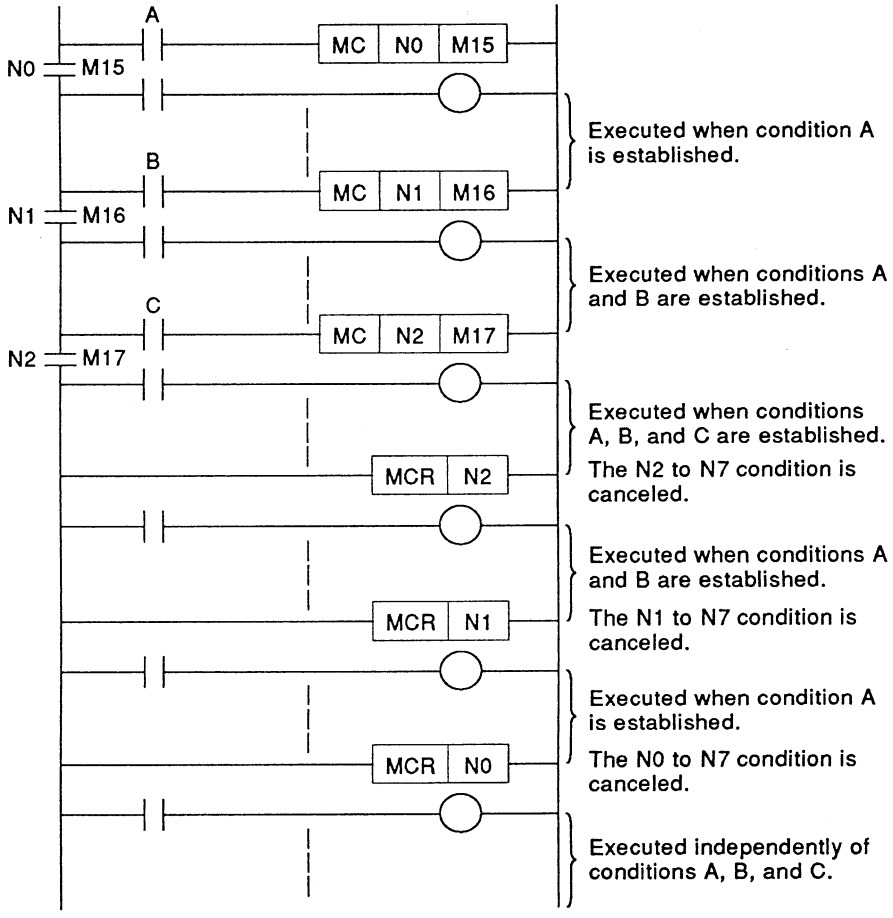
Nesting devices (nesting structures) are used for master control MC instructions.

(1) Nesting N

(a) Master control's nesting (N) is used from the lower numbers. (N0 to N7)
If nesting is not used, the same number's N can be used anytime.

(b) The conditions for turning ON the master controls are as follows:

MC	N0	M15	..... When condition A goes ON
MC	N1	M16	..... When conditions A, B, and C go ON
MC	N2	M17	..... When conditions A and B go ON



(c) The timer and the counter when the master control goes OFF are as follows:
- 100 msec timer and 10 msec timer: Count value becomes 0.
- 100 msec retentive timer: The state of the present count value is retained.
- Counter: The state of the present count value is retained.
- OUT instruction: All are turned OFF.
- SET and SFT instructions: An output that went ON stays ON.

(d) Nesting N numbers are expressed in decimal (0 to 9).

1.2.13 Pointer P

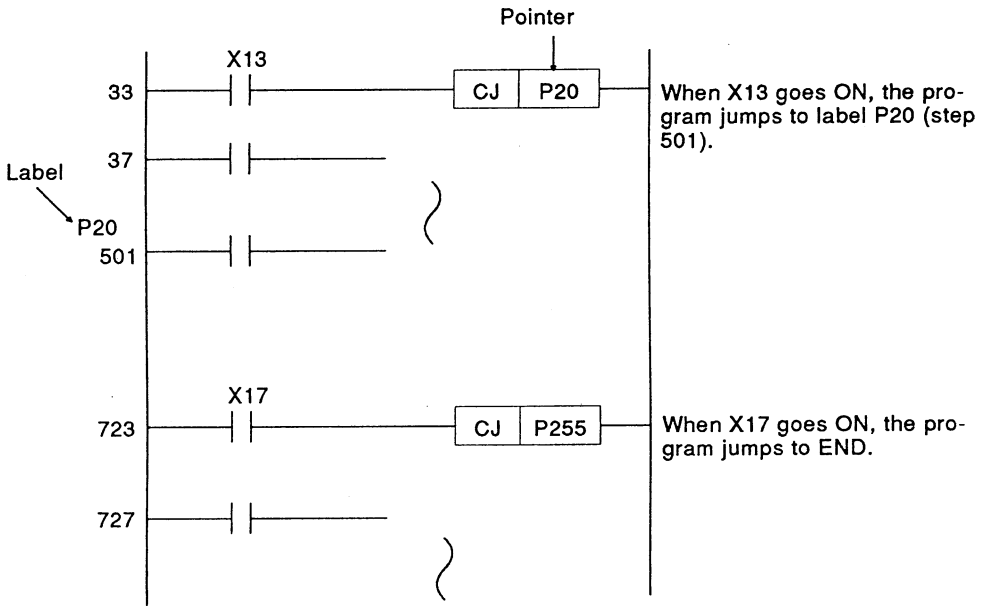
Pointer P shows the jump destination of branch instructions (CJ, SCJ, CALL, JMP). The pointer number put at the head of the program of a jump destination is called a label.

(1) Pointer P

(a) If the same label is used several times, an error occurs.

(b) P255 always shows END.

> P255 can be used as a device for CJ and SCJ instructions, etc. However, it cannot be used as a label. Nor can it be used as a CALL instruction device.



(c) When the CHK instruction is used, P254 is used as a label of the CHK instruction's ladder block. When the CHK instruction is not used, P254 can be used in the same way for P0 to 253.

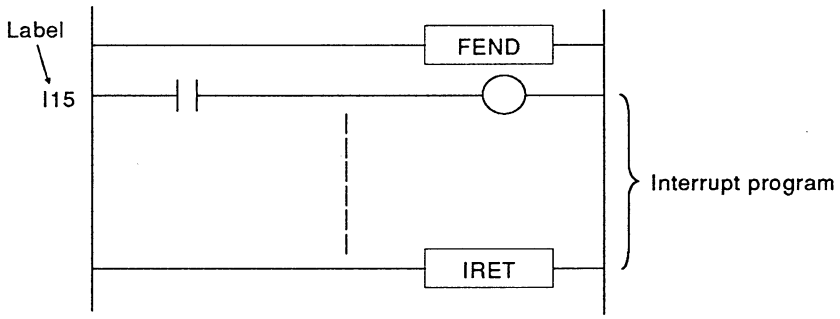
(d) Pointer P numbers are expressed in decimal (0 to 9).

1.2.14 Interrupt pointer I

Interrupt pointer I is used as a jump destination (label) to interrupt the execution of a main program and execute an interrupt program that corresponds to an interrupt factor with the highest priority when an interruption occurs.
However, an EI instruction for interruption enabled is necessary at the head of the main program.

(1) Interrupt pointer I

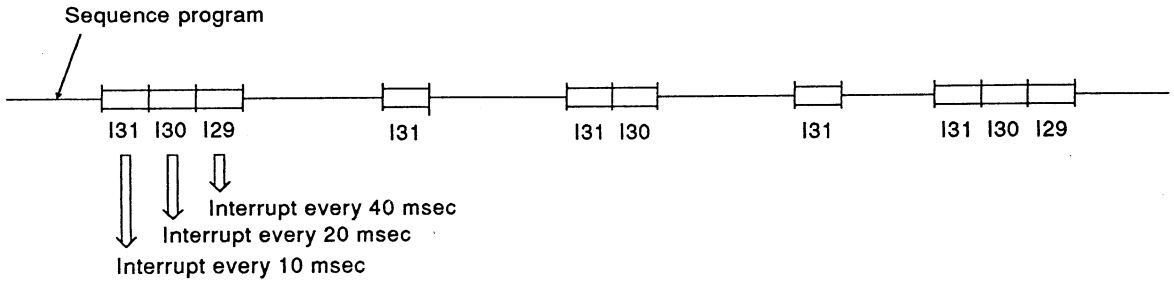
(a) Interrupt pointer I is put at the head of the interrupt program as a label.



(b) The use of interrupt pointers is shown below.

Priorities		Interrupt Pointers	Interrupt Sequence Program Start Factors		
2)	High	I0	Process interrupt	1st point interrupt	
		I1	Unit (AI61)	2nd point interrupt	
		to			
	Low	I15		16th point interrupt	
1)	High	I16	Sequence start occurrence unit	1st unit	The number of the units to be used varies with the CPU module.
		I21	(AD51)	6th unit	
		I22	Unusable		
		to			
	Low	I28			
3)	High	I29	Interrupt every 40 msec		
		I30	Interrupt every 20 msec		
	Low	I31	terrupt every 10 msec		

(c) When I29 to I31 exist in a program, the program jumps to the interrupt program at every interruption time and is executed.



(d) Pointer I numbers are expressed in decimal (0 to 9).

1.3 Parameter Setting

When operating the GPP/PHP, set the parameters prior to the mode selection. The parameter setting refers to the setting of parameters which meet the used system before performing the creation of program. When the parameter setting is not performed (initial status), values shown in the following table are automatically set to the parameters as default values.

Item \ CPU	A0J2CPU Default value	A0J2CPU Parameter setting range	A0J2HCPU Default value	A0J2HCPU Parameter setting range	A1SCPU(S1) Default value	A1SCPU(S1) Parameter setting range	A2CCPU Default value	A2CCPU Parameter setting range	A1CPU, A1NCPU Default value	A1CPU, A1NCPU Parameter setting range
Setting of memory capacity: Main program – Suquence program	3K steps	1 to 7K steps [in units of 1K step]	6K steps	1 to 8K steps [in units of 1K step]	6K steps	0 to 8K steps [in units of 1K step]	6K steps	1 to 8K steps [in units of 1K step]	6K steps	1 to 6K steps [in units of 1K step]
Setting of memory capacity: Main program – Micro-computer program	0K byte	0 to 12K bytes	0K byte	0 to 14K bytes	0K byte	0 to 14K bytes [in units of 2K byte]	0K byte	0 to 14K bytes [in units of 2K bytes]	0K byte	0 to 10K bytes [in units of 2K bytes]
Setting of memory capacity: Sub-program – Sequence program	———	No setting	———	No setting	———	No setting	———	No setting	0K step	No setting
Setting of memory capacity: Sub-program – Micro-computer program	———	No setting	———	No setting	———	No setting	———	No setting	0K byte	No setting
Setting of memory capacity: File register	———	———	0K point	0 to 4K points [in units of 1K point]	0K point	0 to 4K points [in units of 1K point]	0K point	0 to 4K points [in units of 1K point]	0K poimt	No setting
Setting of memory capacity: Comment capacity	64K bytes	0 to 4032 *1 points [in units of 64 points]	0K byte	0, 2 to 64K bytes	0K byte	0 to 1600K points [in units of 64K points]	0K byte	0, 2 to 64K bytes	0K byte	0 to 4032 points *1 [in units of 64 point]
Setting of memory capacity: Sampling trace	No	No setting	No	Yes/No	No	Yes/No	No	Yes/No	No	No setting
Setting of memory capacity: States latch	No	No setting	No	Yes/No	No	Yes/No	No	Yes/No	No	No setting
Latch range setting	1/2 latch	No latch 1/2 latch All latch	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1K point]	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]
Link range specification	———	No setting	———	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to 1FF Output (Y): Y0 to 1FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]
Print title entry	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters
Ladder monitor mode setting	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verity prior to monitor = perfomed/not performed Monitor destination = PC/device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verity prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verity prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verity prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verity prior to monitor = perfomed/not performed Monitor destination = status data /device memory data
Entry cade	No	No setting	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)
MELSECNET/MINI automatic refresh setting	———	———	———	———	———	———	———	———	———	———

	Item \ CPU	A0J2CPU		A0J2HCPU		A1SCPU(S1)		A2CCPU		A1CPU, A1NCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Pameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
	remote terminal setting	—	—	—	—	—	—	Total of remote stations: 64 Online mode: Automatic online returan enabled	Total of remote stations: 1 to 64 Online mode: Automatic online returan enabled /disabled/stop Head station number: 1 to 61 Protocal: MINI /no-protocol	—	—
Auxiliary function setting	Setting of internal relay (M), latch relay (L), step relay (S)	No	By latch range setting	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047
Auxiliary function setting	Watch dog timer	No	No setting	200 ms	10 ms to 2000 ms [in units of 10 ms]	200 ms	10 ms to 2000 ms [in units of 10 ms]	200 ms	10 ms to 2000 ms [in units of 10 ms]	200 ms	10 ms to 2000 ms [in units of 10 ms]
Auxiliary function setting	Timer setting	No	No setting	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100ms, 10ms, retentive timers [in units of 8 points]
Auxiliary function setting	I/O assignment	No	No setting	—	0, 16, 32, 48, 64 points • Input (X) unit • Output (Y) unit • Special unit • Empty slot [in unit of 16 points]	—	0, 16, 32, 48, 64 points • Input (X) unit • Output (Y) unit • Special unit • Empty slot [in unit of 16 points]	—	0, 16, 32, 48, 64 points • Input (X) unit • Output (Y) unit • Special unit • Empty slot [in unit of 16 points]	—	0, 16, 32, 48, 64 points • Input (X) unit • Output (Y) unit • Special unit • Empty slot [in unit of 16 points]
Auxiliary function setting	Remote RUN/PAUSE setting	No	No setting	—	X0 to 1FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	—	X0 to FF(A1SCPU) X0 to 1FF (A1SCPU-S1) [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	—	X0 to 1FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	—	X0 to FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]
Auxiliary function setting	RUN mode at error	No	No setting	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]
Auxiliary function setting	Annunclator display mode	No	No setting	No	No setting	No	No setting	No	No setting	No	No setting
Auxiliary function setting	STOP → RUN output mode	No	No setting	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation
Auxiliary function setting	Counter setting (Interrupt counter)	No	No setting	—	C0 to 255 [in units of 8 points]	—	C0 to 255 [in units of 8 points]	—	No setting	—	C0 to 255 [in units of 8 points]
Auxiliary function setting	I/O control mode	Direct fixed		Can be changed direct/refresh with switch. Set for direct mode before delivery.		Can be changed direct/refresh with switch. Set for direct mode before delivery.		Refresh fixed		A1 and A2CPU is set for direct mode. A1NCPU and A2NCPU can be changed direct/refresh with switch. Set for direct mode befor delivery.	

POINTS

(1) *1: When the A0J2 is used, only 95 points of comment data (F0 to F94) can be transferred. When the A1CPU is used, only 128 points (F0 to F127) can be transferred.

(2) After setting each parameter, always press [END]. If another screen is desplayed without pressing [END], the old data is valid and the new data is not entered. To return to the preceding screen, also press [END].

Item	A2CPU, A2NCPU Default value	A2CPU, A2NCPU Parameter setting range	A2ACPU Default value	A2ACPU Parameter setting range	A3CPU, A3NCPU Default value	A3CPU, A3NCPU Parameter setting range	A3HCPU, A3MCPU Default value	A3HCPU, A3MCPU Parameter setting range	A3ACPU Default value	A3ACPU Parameter setting range
Setting of memory capacity – Main program – Suqu-ence program	6K steps	1 to 14K steps [in units of 1K step]	6K steps	1 to 14K steps [in units of 1K step]	6K steps	0 to 30K steps [in units of 1K step]	6K steps	0 to 30K steps [in units of 1K step]	6K steps	0 to 30K steps [in units of 1K step]
Setting of memory capacity – Main program – Micro-computer program	0K byte	0 to 26K bytes [in units of 2K step]	———	No setting	0K byte	0 to 58K bytes [in units of 2K bytes]	0K byte	0 to 58K bytes [in units of 2K bytes]	———	No setting
Setting of memory capacity – Sub-program – Sequ-ence program	0K step	No setting	———	No setting	0K step	0 to 30K steps [in unites of 1K step]	0K step	0 to 30K steps [in units of 1K step]	0K step	1 to 30K steps [in units of 1K step]
Setting of memory capacity – Sub-program – Micro-computer program	0K byte	No setting	———	No setting	0K byte	0 to 58K bytes [in units of 2K bytes]	0K byte	0 to 58K bytes [in units of 2K bytes]	———	No setting
Setting of memory capacity – File register	0K point	0 to 4K points [in units of 1K point]	0K point	0 to 8K points [in units of 1K point]	0K point	0 to 8K points [in units of 1K point]	0K point	0 to 8K points [in units of 1K point]	0K point	0 to 8K points [in units of 1K point]
Setting of memory capacity – Comment capacity	0K byte	0 to 4032 points [in units of 64 points]	0K byte	0, 2 to 64K bytes	0K byte	0 to 4032K points [in units of 64 points]	0K byte	0 to 4032K points [in units of 64 points]	0K byte	0, 2 to 64K bytes
Setting of memory capacity – Sampling trace	No	Yes/No	No	No setting	No	Yes/No	No	Yes/No	No	No setting
Setting of memory capacity – States latch	No	Yes/No	No	No setting	No	Yes/No	No	Yes/No	No	No setting
Latch range setting	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]	———	B0 to FFF T0 to 255, 256 to 2047 C0 to 255, 256 to 1023 D0 to 6143 W0 to FFF [in units of 1 point]	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]	———	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF [in units of 1 point]	———	B0 to FFF T0 to 255, 256 to 2047 C0 to 255, 256 to 1023 D0 to 6143 W0 to FFF [in units of 1 point]
Link range spacification	———	Number of link stations: 1 to 64 Input (X): X0 to 1FF Output (Y): Y0 to 1FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to 1FF Output (Y): Y0 to 1FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to 7FF Output (Y): Y0 to 7FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to 7FF Output (Y): Y0 to 7FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]	———	Number of link stations: 1 to 64 Input (X): X0 to 7FF Output (Y): Y0 to 7FF Link relay (B): B0 to 3FF Link registor (W): W0 to 3FF Monitor time: 10 ms to 2000 ms [in units of 10 ms]
Print title entry	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters	———	128 alphanumeric and special characters
Ladder monitor mode setting	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verify prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verify prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verify prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verify prior to monitor = perfomed/not performed Monitor destination = status data /device memory data	Program verify prior to monitor = not Perfomed Monitor destination = PC	Program verify prior to monitor = perfomed/not performed Monitor destination = status data /device memory data
Entry cade	———	6digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)	———	6 digits of hexadecimal number (0 to 9, A to F)
MELSECNET/MINI automatic refresh setting	———	———	Number of modules: 0	Number of modules: 0 to 8	———	———	———	———	Number of modules: 0	Number of modules: 0 to 8
Remote terminal setting	———	———	———	———	———	———	———	———	———	———
Auxiliary function setting – Setting of internal relay (M), latch relay (L), step relay (S)	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 M2048 to 8191 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 M2048 to 8191 L1000 to 2047	M/L/S0 to 2047
Auxiliary function setting – Watch dog timer	200 ms	10 ms to 2000 ms [in units of 10 ms]	200 ms		200 ms	10 ms to 2000 ms [in units of 10 ms]	200 msec fixed		200 msec fixed	
Auxiliary function setting – Timer setting	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	Points used: 256 100 ms: T0 to 199 10 ms: T200 to 255	T0 to 2047, setting of 100 ms, 10 ms,or retentive timers [in units of 8 points; for T256 and over, 16 points]	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	100 ms: T0 to 199 10 ms: T200 to 255	Setting of 100 ms, 10 ms, retentive timers [in units of 8 points]	Points used: 256 100 ms: T0 to 199 10 ms: T200 to 255	T0 to 2047, setting of 100 ms, 10 ms, or retentive timers [in units of 8 points; for T256 and over, 16 points]

	CPU / Item	A2CPU, A2NCPU Default value	A2CPU, A2NCPU Parameter setting range	A2ACPU Default value	A2ACPU Parameter setting range	A3CPU, A3NCPU Default value	A3CPU, A3NCPU Parameter setting range	A3HCPU, A3MCPU Default value	A3HCPU, A3MCPU Parameter setting range	A3ACPU Default value	A3ACPU Parameter setting range
Auxiliary function setting	I/O assignment	———	0, 16, 32, 48, 64 points [• Input (X) unit • Output (Y) unit • Special unit • Empty slot in units of 16 points]	———	0, 16, 32, 48, 64 points [• Input (X) unit • Output (Y) unit • Special unit • Empty slot in units of 16 points]	———	0, 16, 32, 48, 64 points [• Input (X) unit • Output (Y) unit • Special unit • Empty slot in units of 16 points]	———	0, 16, 32, 48, 64 points [• Input (X) unit • Output (Y) unit • Special unit • Empty slot in units of 16 points]	———	0, 16, 32, 48, 64 points [• Input (X) unit • Output (Y) unit • Special unit • Empty slot in units of 16 points]
	Remote RUN/PAUSE setting	———	X0 to 1FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	———	X0 to 1FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	———	X0 to 7FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	———	X0 to 7FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]	———	X0 to 7FF [Only 1 point can be set for RUN contact. setting of only pause contact is not allowed.]
	RUN mode at error	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]	Continuation [• Fuse blow • Operation error] Stop [• I/O unit verify error • Special function • Unit operation error]	Stop/continuation [• Fuse blow • Operation error • I/O unit verify error • Special function • Unit operation error]
	Annunciator display mode	No	No setting	No	No setting	No	Display Yes/No	No	Display Yes/No	F number indication	Switching indication of F number and comment
	STOP → RUN output mode	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is regenerated	Output of status prior to STOP or result one scan after operation
	Counter setting (Interrupt counter)	———	C0 to 255 [in units of 8 points]	256 points	C0 to 1023 [Whether C224 to C255 are used or not can be set to corresponding interrupt pointers I]	———	C0 to 255 in units of 8 points	C0 to 255 Whether C224 to C255 are used or not can be set to corresponding interrupt pointers I		256 points	C0 to 1023 [Whether C224 to C255 are used or not can be set to corresponding interrupt pointers I]
	I/O control mode	A1, A2CPU is set for direct mode. A1N, A2NCPU can be changed direct/refresh with switch. Set for direct mode before delivery.		Refresh fixed		A3CPU is set for direct mode. A3NCPU can be changed direct/refresh with switch. Set for direct mode before delivery.		Input/output in direct mode	Input/output in direct mode Input in direct mode/output in refresh mode Input/output in refresh mode	Refresh fixed	

REMARK

Due to the capacity of CPU memory and memory cassette, it is dometimes impossible to set the capacity for programs, file registers and comments all at the maximum value.

2. ALLOCATION OF I/O NUMBERS

2.1 I/O Numbers of a Compact Type A0J2 and A0J2H

In the case of compact types, the X/Y numbers are decided automatically by the I/O module's setting numbers.
If an A6GPP is used, I/O allocation cannot be done.

Since the allocation of I/O numbers is one of the necessary conditions for configuring a system, if the allocation is wrong, it will cause a malfunction. This section explains the allocation of an I/O module's I/O numbers.

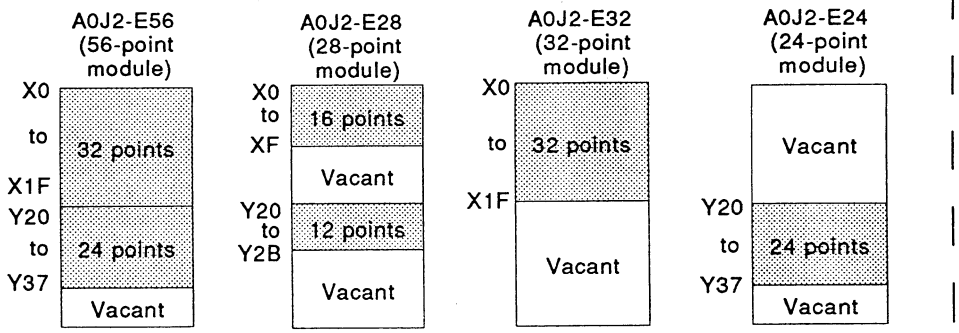
(1) Each I/O module and extension unit slot occupies 64 points. The allocations of input (X) and output (Y) are as follows.

(a) Input (X) ..... First 32 points

(b) Output (Y) ..... Latter 32 points

Example

When the I/O module setting number is 0, the I/O numbers of each I/O module are as follows:



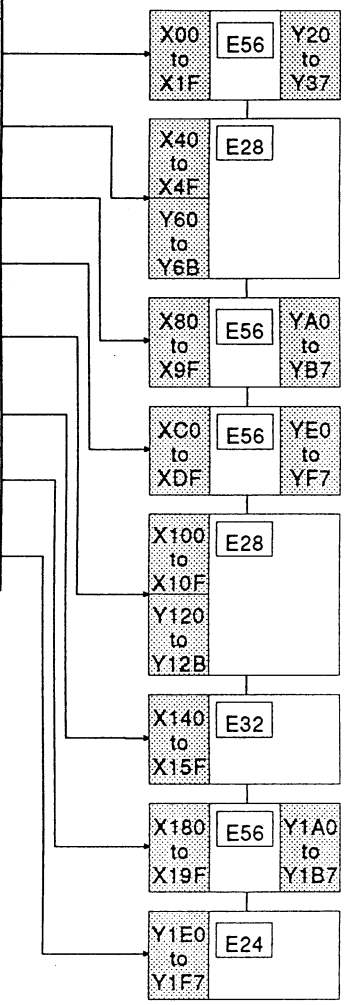
(2) The head I/O numbers of an I/O module is provided as follows in accordance with the I/O module setting numbers:

Setting	0	1	2	3	4	5	6	7
Head input number	X00	X40	X80	XC0	X100	X140	X180	X1C0
Head output number	Y20	Y60	YA0	YE0	Y120	Y160	Y1A0	Y1E0

(3) Allocations of I/O numbers are not done in the order of a connection of an extension cable connections. They are allocated in the order of I/O module setting numbers.

Example of I/O number allocations in an A0J2 or A0J2HCPU system

I/O Module No.	I/O Number
0	X00 to X1F Y20 to Y3F
1	X40 to X5F Y60 to Y7F
2	X80 to X9F YA0 to YBF
3	XC0 to XDF YE0 to YFF
4	X100 to X11F Y120 to Y13F
5	X140 to X15F Y160 to Y17F
6	X180 to X19F Y1A0 to Y1BF
7	X1C0 to X1DF Y1E0 to Y1FF



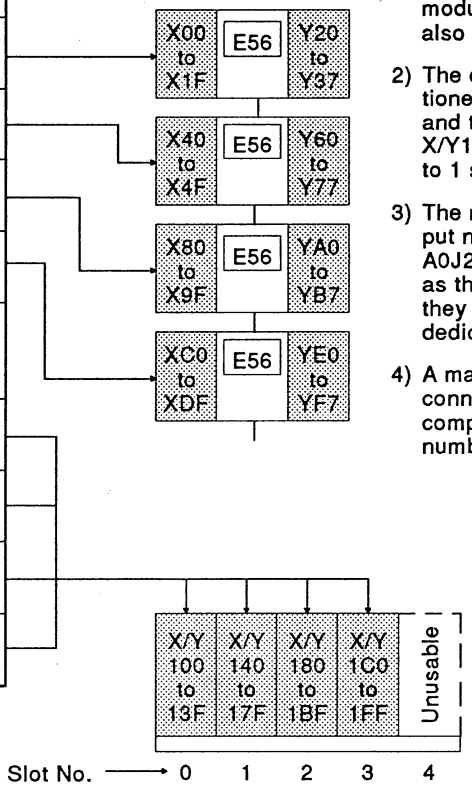
1) The number of occupied input/output points per module is 64 points.
2) The I/O number is decided by the I/O module number (0 to 7). Section 3.2.2 of the User's Manual (I/O module) gives details about how to set I/O module numbers.
3) Max. 8 I/O modules can be connected.
4) Since the number of occupied I/O points per module is 64 points, when 24 points are used, 40 points are unused. However, it is not necessary to change a currently used I/O number even if the I/O module is exchanged in the future.
5) The numbers that correspond to the input numbers and unused numbers (32 points of the latter half in the case of a special module) can be used instead of the internal memory (M). However, they cannot be used in the case of a dedicated input module.
6) Make sure the same I/O module number is not used more than once in the system, since doing so causes a malfunction.
7) The I/O module numbers are 0 to 7. However, it is not necessary to allocate I/O module numbers in order. I/O numbers are determined by I/O module numbers as shown to the left. However, Mitsubishi recommends setting consecutive numbers from the standpoint of I/O numbers.

Fig. 2.1 Allocation Example

(4) When an extension base unit is used, the I/O numbers start from X/Y100.

Example of I/O number allocation using an extension base unit composite system

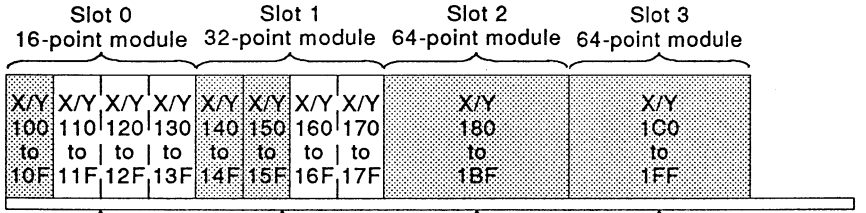
I/O Module No.	I/O Number
0	X00 to X1F Y20 to Y3F
1	X40 to X5F Y60 to Y7F
2	X80 to X9F YA0 to YBF
3	XC0 to XDF YE0 to YFF
Slot No. on the extension base unit	I/O number
0	X100 to X13F Y100 to Y13F
1	X140 to X17F Y140 to Y17F
2	X180 to X1BF Y180 to Y1BF
3	X1C0 to X1FF Y1C0 to Y1FF



1) The number of occupied module inputs/outputs is 64 points. (The number of occupied inputs/outputs of the I/O module in an extension base unit is also 64 points.)
2) The extension base unit is always positioned in the final stage of the system, and the I/O number always begins with X/Y100. (The number of stages is set to 1 stage.)
3) The numbers that correspond to an input number and unused numbers in an A0J2 I/O module system can be used as the internal memory (M). However, they cannot be used in the case of a dedicated input module.
4) A max. of 4 A0J2 I/O modules can be connected in an extension base unit composite system. Set the 1/O unit number to 0 to 3.

Restrictions with an extension base unit

1) Only slots 0 to 3 can be used in an extension base unit.
2) One slot occupies 64 points independently of the number of utilized I/O module points and empty slots. When an input module is used, the corresponding numbers (all the corresponding numbers for 64 points) cannot be used instead of the internal memory.
3) Pay attention to the following when a 64-point I/O module is not used (e.g. when a 16-point or 32-point module are used).



- When a 64-point module is used, there are no restrictions.
- When a 32-point module is used, the latter 32 points are not used. However, in reality, the first 32 points and latter 32 points are lapped during CPU access. Therefore, if an I/O number in the latter half is used in the program incorrectly, the A0J2/A0J2H behaves as if an I/O number in the lapped first half has been accessed. For example, 160 is lapped by 140, and 170 is lapped by 150.
- When a 16-point module is used, the latter 48 points are not utilized. The A0J2/A0J2H regards those 48 points as a lap of 4 16-point modules. For example, if 110, 120 or 130 is accessed, it behaves as if 100 had been accessed. Always be sure to use actual I/O numbers in the program. X/Y100-10F are the actual I/O numbers in the example on the left.

Fig. 2.2 Example of I/O Number Allocations in a Composite System

2.2 A2CCPU I/O Allocations

The A2CCPU uses I/O numbers to control communications with I/O modules and remote terminals. The I/O numbers are allocated with X/Y0 to X/Y1FF in the order of station numbers set by using the station number setting switch on each module. Note that the I/O number allocations are not executed in the order I/O modules and remote terminal modules are connected.

(1) Station numbers and I/O number allocations

Each station is allocated in 8-point units. Stations 1 to 64 can be set. The following table shows the correspondence between station number settings and I/O number allocations.

Table 2.1 Correspondence between Station Numbers and I/O Numbers

Station No.	I/O Number	Station No.	I/O Number	Station No.	I/O Number	Station No.	I/O Number
1	X/Y0 to 7	17	X/Y80 to 87	33	X/Y100 to 107	49	X/Y180 to 187
2	X/Y8 to F	18	X/Y88 to 8F	34	X/Y108 to 10F	50	X/Y188 to 18F
3	X/Y10 to 17	19	X/Y90 to 97	35	X/Y110 to 117	51	X/Y190 to 197
4	X/Y18 to 1F	20	X/Y98 to 9F	36	X/Y118 to 11F	52	X/Y198 to 19F
5	X/Y20 to 27	21	X/YA0 to A7	37	X/Y120 to 127	53	X/Y1A0 to 1A7
6	X/Y28 to 2F	22	X/YA8 to AF	38	X/Y128 to 12F	54	X/Y1A8 to 1AF
7	X/Y30 to 37	23	X/YB0 to B7	39	X/Y130 to 137	55	X/Y1B0 to 1B7
8	X/Y38 to 3F	24	X/YB8 to BF	40	X/Y138 to 13F	56	X/Y1B8 to 1BF
9	X/Y40 to 47	25	X/YC0 to C7	41	X/Y140 to 147	57	X/Y1C0 to 1C7
10	X/Y48 to 4F	26	X/YC8 to CF	42	X/Y148 to 14F	58	X/Y1C8 to 1CF
11	X/Y50 to 57	27	X/YD0 to D7	43	X/Y150 to 157	59	X/Y1D0 to 1D7
12	X/Y58 to 5F	28	X/YD8 to DF	44	X/Y158 to 15F	60	X/Y1D8 to 1DF
13	X/Y60 to 67	29	X/YE0 to E7	45	X/Y160 to 167	61	X/Y1E0 to 1E7
14	X/Y68 to 6F	30	X/YE8 to EF	46	X/Y168 to 16F	62	X/Y1E8 to 1EF
15	X/Y70 to 77	31	X/YF0 to F7	47	X/Y170 to 177	63	X/Y1F0 to 1F7
16	X/Y78 to 7F	32	X/YF8 to FF	48	X/Y178 to 17F	64	X/Y1F8 to 1FF

(2) Correspondence of occupied points and station numbers

(a) If the number of I/O module and remote terminal module I/O points is 8 or more, one module occupies several consecutive station numbers.
Station numbers occupied by one module cannot be set to other modules.

(b) Set the station numbers to I/O modules and remote terminal modules so that the numbers are consecutive.
When modules which occupy 8 or more points per module are used, set the head station number of the station numbers occupied by the modules as the station number of the module.

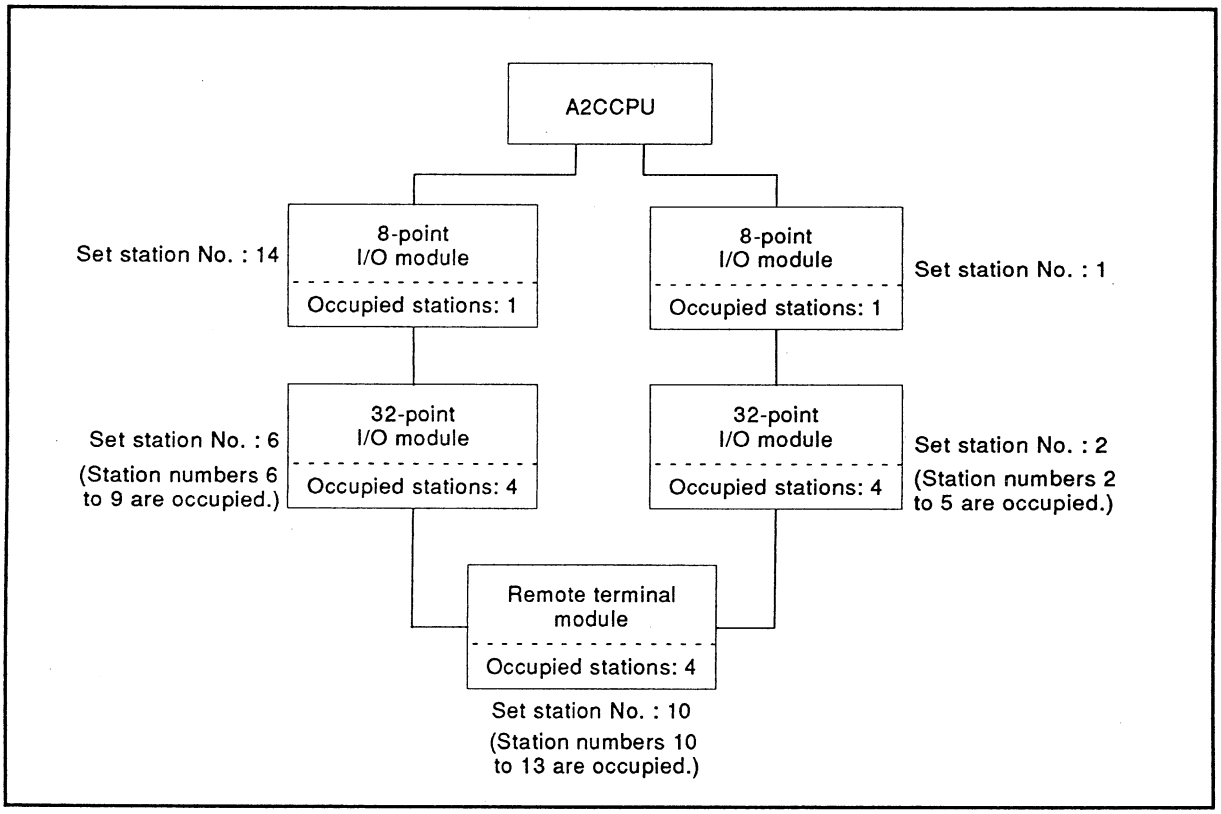


Fig. 2.3 Station Number Setting Example

POINTS

(1) Setting the same station number may cause a wrong input or output.
When setting a station number, be careful not to use the same station number or a lapped station number when taking the number of occupied inputs/outputs into consideration.

(2) If a station number is skipped, the skipped station number becomes a faulty station, and then M9061 goes ON.
The ERR LED on the front of the A2C lights.

2.3 I/O Numbers of a Building Block Type CPU

When a building block type (A1S, A1 to A3 type) CPU is used, I/O modules can be allocated anywhere.
When an I/O module is allocated to the base, the I/O numbers are set automatically. X or Y numbers must be used in the program.
I/O numbers can be divided into "parent numbers" OO (determined by the number of I/O points of the module used in each slot) and "child numbers" O (hexadecimal subdivisions of parent numbers) as shown in the following example.

Example) Input: X 12 F

Module's one hexadecimal character (child number)

One or two hexadecimal characters decided by the number of module I/O points (parent number)

I/O numbers in the case of 16-point and multi-point modules are explained below.

2.3.1 When only a 16-point module is used

(1) Main base unit's I/O numbers

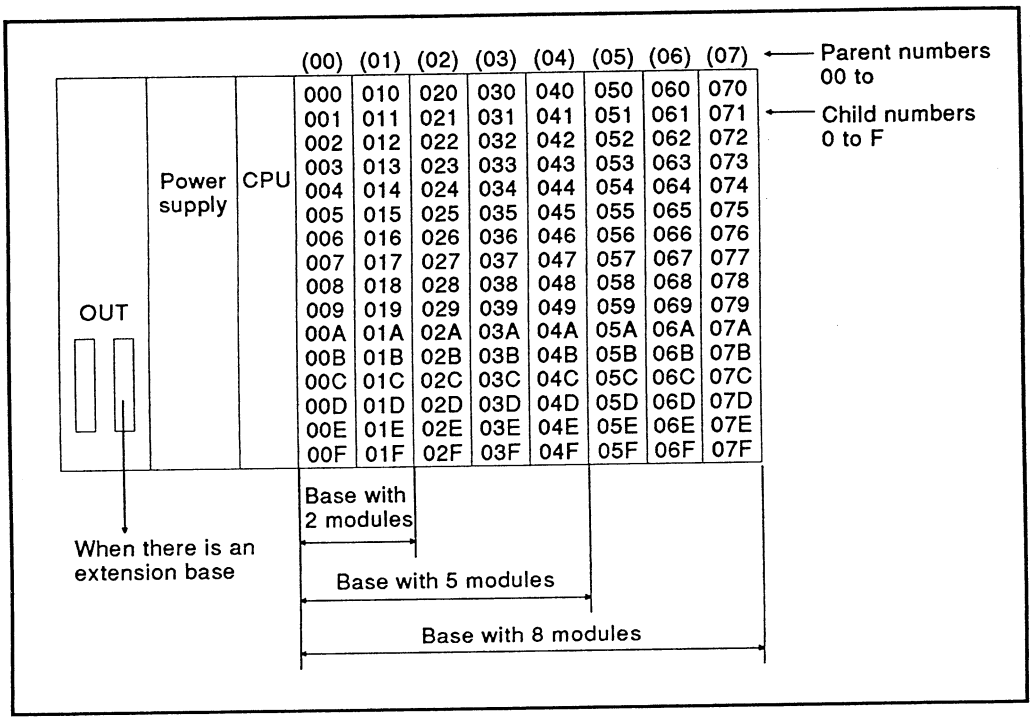


Fig. 2.4 Extension Bases (16-Point Module)

Modules to the right of the CPU on the base unit are allocated in order to parent numbers 00 and 01. The hexadecimal numbers of each module are the child numbers.
For example, when input module X is allocated to parent number 00, the input numbers become X000, X001, and X002, X003....X00F.
When output module Y is allocated to parent number 02, the output numbers become Y020, Y021, Y022, Y023....Y02F.
In the case of X001, it is displayed as X1 (the higher 0 is omitted).
The blank which has no allocated module occupies 16 points. Therefore, this number is not used. If a module is allocated to the blank, the number is used.
When temporary memory M runs short. A blank virtual Y can be used as a temporary memory. However, be careful the number is not repeated if an output module is allocated later. In such a case, the number of virtual Y used as the temporary memory must be changed.

(2) I/O numbers of a extension base unit

When 16-point modules are used independently of a main base unit (See Fig. 2.5), the module furthest to the left of the first extension base unit is considered parent number 08 and numbers are allocated sequentially. The second extension base starts from parent number 10 and the third extension base starts from parent number 18. The advantage here is that the extension base I/O numbers do not change even if a main base unit with 2, 5, or 8 modules is used.
There are extension bases with 5 modules and with 8 modules, as shown in Fig. 2.6. When either is used, the next stage's extension base number does not change and starts from parent number 10 or parent number 18.
256 I/O points are displayed in hexadecimal from 000 to 0FF, and 512 points are displayed in hexadecimal from 000 to 1FF.

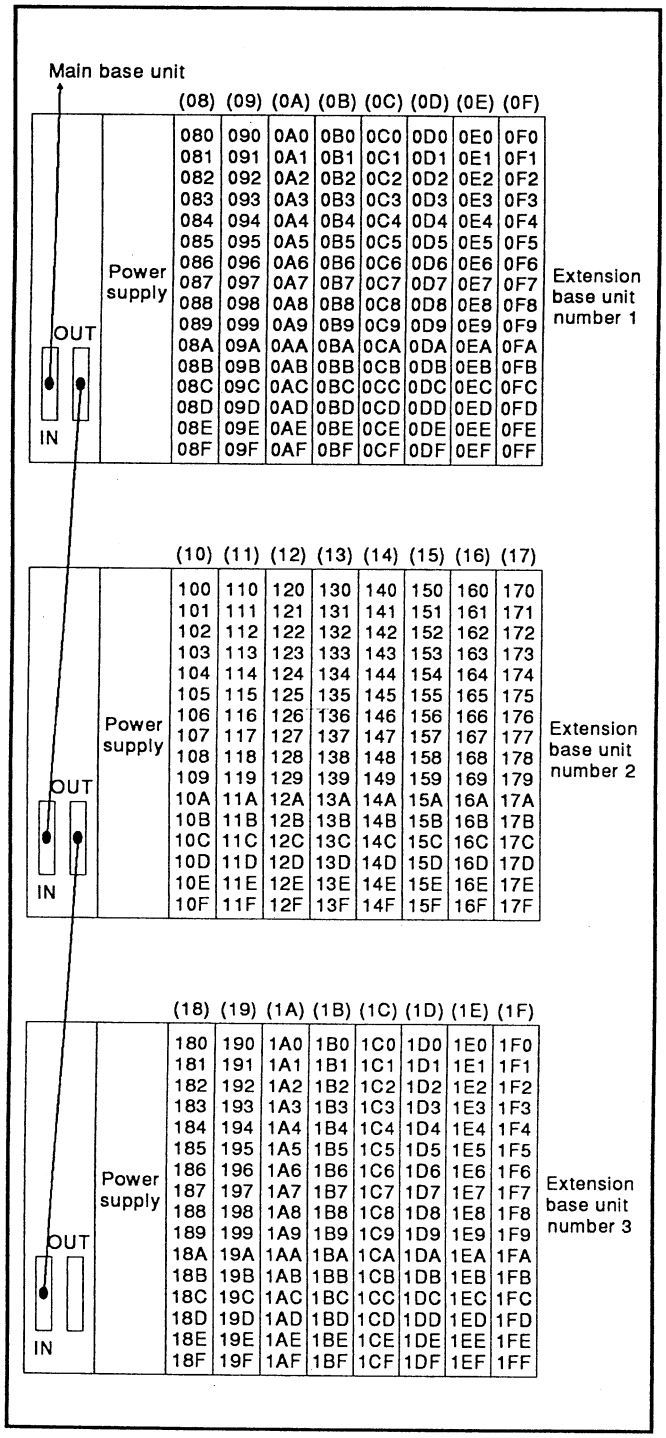


Fig. 2.5 Extension Base Units (16-point)

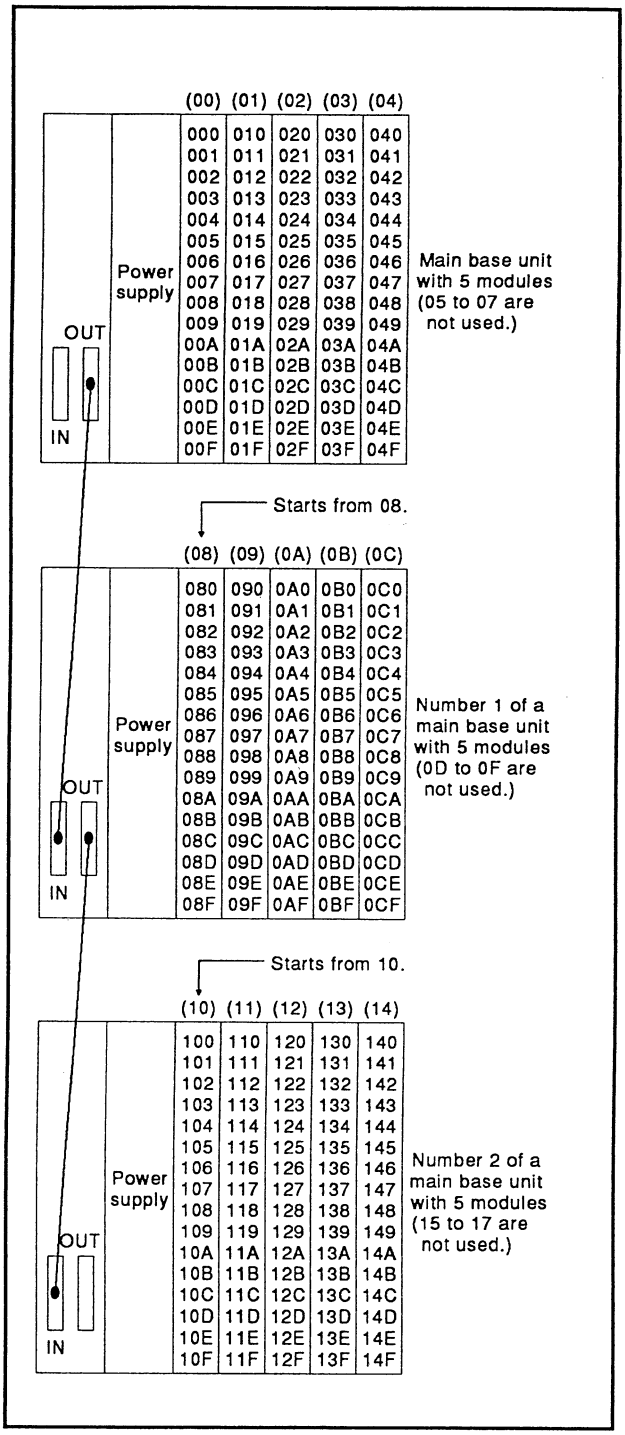


Fig. 2.6 Combination Examples

2.3.2 When 32-point and 64-point modules are used

The basic idea is same as when 16-point modules are used.
When using 16-point modules, 16 points must be allocated to the base module 1. When using 32-point modules, 32 points must be allocated to the module 1, and continuous numbers are utilized by shifting the numbers. When using 64-point modules, 64 points must be allocated to module 1. In the case of a special module, pay attention to the number of occupied I/Os and the allocation.
Allocation examples are given below.

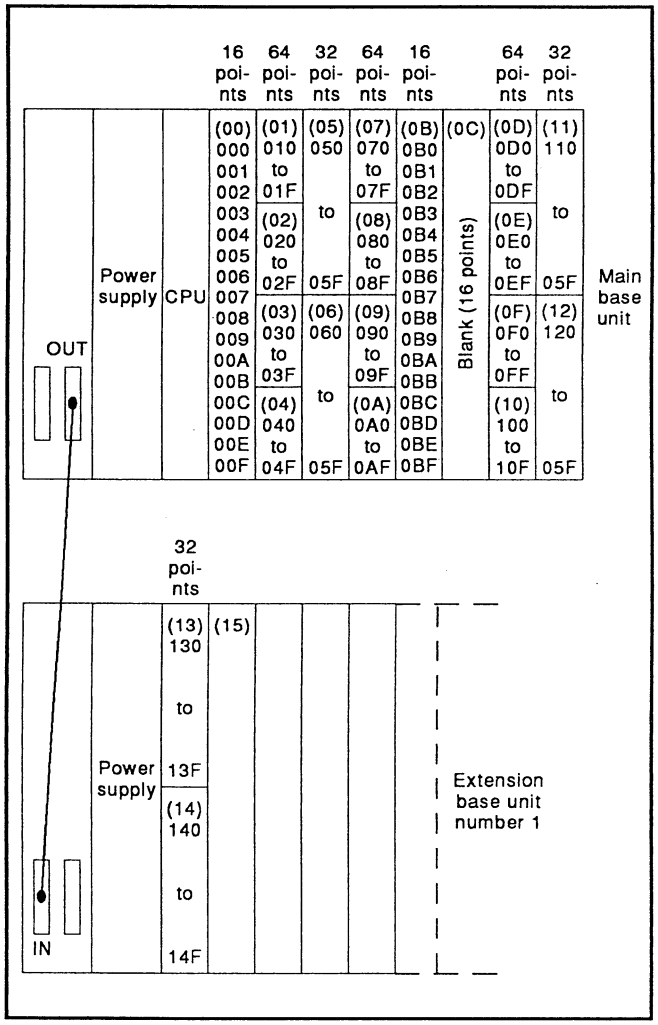


Fig. 2.7 Main Base Unit Example (Multi-Point Module)

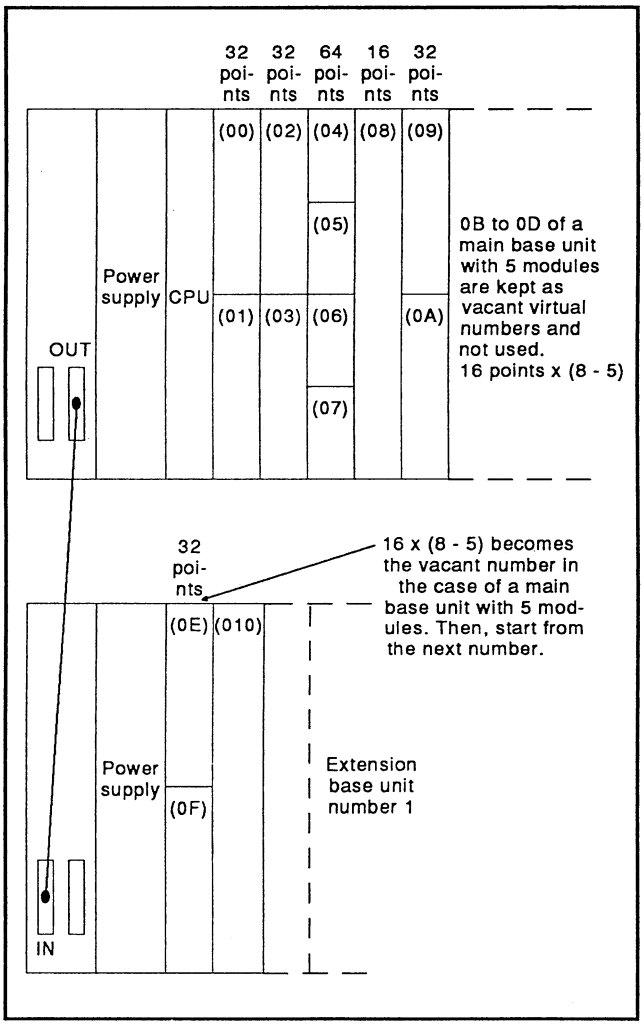


Fig. 2.8 Combination Example (Multi-Point Module)

In the example in Fig. 2.7, parent number 0 is allocated to the 16-point module.
If the module in the next slot is allocated 64 points, numbers 010 to 04F are occupied. As shown below, consecutive hexadecimal numbers utilize the same method.
16 points are allocated for the empty slot in which a module is not allocated (parent number 0C).

(1) I/O numbers of an extension base

The extension base in Fig. 2.7 starts with parent number 13 consecutively from the numbers of the main base unit.
However, as shown in Fig. 2.8, in the case of a main base unit with 5 modules, I/O numbers skip a number of points (16 X 3). The 3 indicates the difference between main base units with 8 modules and main base units with 5 modules.
Therefore, the I/O number must be after parent number 08 certainly, because 16 points are allocated to a virtual slot.
In the case of an extension base with 5 modules, the I/O number of the next extension base skips the number of points (16 X 3). The 3 indicates the difference between extension base units with 8 modules and extension base with 5 modules.

(2) Blank and additional modules

The blank in which a module is not installed occupies 16 points. When a 32-point or 64-point module is added to parent number 0C after creating the program of Fig. 2.7, all I/O numbers on the right side of the module shift to the back. Therefore, be very careful when a program is changed. When a 64-point module is installed in blank parent number 0C, parent numbers 0C, 0D, 0E, and 0F are used in this slot, and parent number 0D on the right side becomes module 10. Therefore, all the following I/O numbers must be changed. If a 16-point module is added to parent number 0C, the I/O numbers do not change.
Therefore, from the viewpoint of the fact, a many-point module can be added like this, and the number of occupied inputs/outputs cannot be changed between 32 points and 64 points. However, there are following two methods:

(a) Dummy module (AG62)

A dummy module is a kind of a blank cover. However, it has the number of points setting switch. 16 points or 64 points can be secured in advance by using this switch. If the use of an additional module is expected, insert a dummy module into the base unit to which the number of points is set.

(b) Adding a module after the final base module.

If a module is added after the final module allocated to the base, the existing I/O numbers do not change. In this case, do not prepare a blank in the middle.

2.3.3 I/O allocation by using parameter setting

I/O numbers can be allocated by the GPP's parameter setting.

(1) I/O allocation is done for the following three reasons:

(a) If there is an empty slot in the base, 16 points are usually occupied. But 16 points of the I/O number of points can be saved by setting 0 points by using I/O allocation, thus enabling the I/O slot to be effectively put to practical use.

(b) When there is an empty slot, it is possible to reserve the number of points without a dummy module by setting 32 points, 48 points, or 64 points to expand the system in the future.

(c) By setting the I/O allocation, even when a faulty module is removed, the I/O numbers do not change. If a 32-point module is removed when I/O numbers are not allocated, for example, number of occupied inputs/outputs becomes 16 points, and the numbers change.

(2) I/O allocation by an A6GPP

(a) 0, 16, 32, 48, or 64 points can be allocated to a slot.
The number of vacant points (0, 16, 32, 48, or 64 points) (S), the number of input points (16, 32, 48, or 64 points) (X), the number of output points (16, 32, 48, or 64 points) (Y), or the number of special-function points (16, 32, 48, or 64 points) (F) are allocated. I/O numbers are allocated by the set number of points.

(b) Allocate the number of points that is the same as the number of installation points in the slot where a special-function module is installed by setting special function (F). If the setting is different, an error occurs.

(c) The number of installation points is allocated to the slot that was not set.

(d) If a number of points that is fewer than the number of installation points of an I/O module is set, the number of actually utilized I/O points decreases.

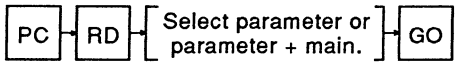
Example)
Installation: 32 input points, I/O allocation: If 16 input points have been allocated, the 16 points in the latter half of an input module cannot be used.

(e) If the number of points that has been set is greater than the number of installation points of the I/O module, the number of points that exceeds the number of installation points becomes the number of dummy points.

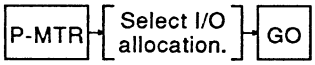
(f) If vacant (S) is set for a slot which is installed to the I/O module, the I/O module becomes unusable.

(3) How to read I/O allocations using an A6GPP
I/O number allocations can be read using an A6GPP by the following key operations:

(a) To read PC parameters



(b) To read only the parameter's I/O allocations



If this list is blank, I/O numbers have not been allocated by the A6GPP.

(4) Peripheral devices other than an A6GPP
I/O numbers cannot be allocated by A6PU, A7PU, and an A7PUS.
I/O numbers can be allocated by A6HGP, A6PHP, and an A7PHP.

3. INSTALLATION ENVIRONMENT

3.1 Installation Environment

Never install the CPU system in the following environments:

(1) Locations where the ambient temperature is outside the range of 0 to 55 °C.

(2) Locations where the ambient humidity is outside the range of 10 to 90 %RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive and/or combustible gasses.

(5) Locations where there is a high level of conductive powder (such as dust and iron filings, oil mist, salt, and organic solvents).

(6) Locations exposed to direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

(8) Locations where vibration and shock are directly transmitted to the main module.

3.2 Electronic Environment

(1) The fluctuation range of a 100 V or 200 V power supply must be within +10 % to -15 %.
If the ambient temperature is above 50 °C, use a PC at approx. 100 % voltage.

(2) Momentary power failure times
If not longer than 20 msec, operations are continued.

(3) Power supply waveform distortion
It should be a sine waveform, and the distortion factor should be within 5 %. Pay particular attention to the power capacitor and the rectifier.

(4) Wiring should be as far as possible from high-tension wires and large current lines.
When parallel, intervals should be 100 mm or more.

(5) Do not store PCs and noise generators on the same board.
Store high-frequency devices, inverters, electrical discharge machines, etc. on a separate board, and store them as far as possible from PCs. Wiring should be separated.

4. HANDLING AND MOUNTING

4.1 Handling

Since the electronic parts which are installed on the printed circuit board are influenced by static electricity, pay special attention to the following when handling a printed circuit board directly:

- Ground the human body or work bench.
- Do not directly touch the conducting area and electric parts of a product.

(1) Handling modules

- Secure each module to the base unit correctly.
- Do not insert or remove a module during power ON (doing so might cause a wrong input).
- Do not touch the gold plating on a printed circuit board (doing so will cause a contact fault).

(2) Handling the memory

- When mounting the memory, be sure to fit the memory in the proper direction as indicated on the socket.
  Also, make sure the connectors are properly set and do not protrude.
- Do not touch the memory leads. Also, make sure the leads are not bent.

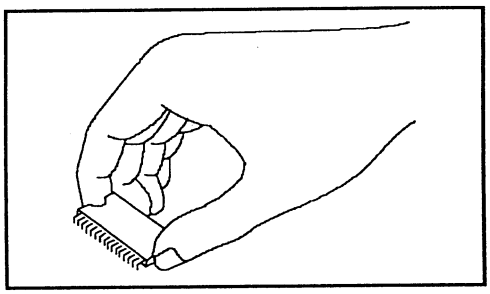


Fig. 4.1 How to Hold the Memory

- When removed or stored, always put the memory in the supplied case.
- Never place the memory on metal, which may allow current flow, or on any object (such as wood, plastic, vinyl, fiber, cable, or paper) which is charged with static electricity,.

EP-ROM memory

- Make every effort to keep the glass face and leads of the ROM free from finger smudges and oils. If any does get on the ROM, wipe it off with alcohol.
- A mask tape is attached to the ROM to prevent ultraviolet rays from erasing programs.
  When erasing a program, peel off this mask tape. Several minutes' direct exposure to sunlight will erase programs. Longer exposure (an hour or more) to light from a fluorescent lamp will erase programs.

IC-RAM memory

- If this is removed during program writing, the program is erased.

4.2 PC Installation

This section explains how to install a PC and gives precautions to take when doing so.

4.2.1 Mounting instructions

Explanation is given to the instructions for mounting the PC to a panel, etc.

(1) To improve ventilation or facilitate the replacement of unit, provide 80 mm (3.15 in.) or more the clearance around the PC. (A1SCPU: 30 mm (1.18 in.)or more)

(2) Do not mount the base unit vertically or horizontally to allow ventilation.

(3) Ensure that the base unit mounting surface is uniform to prevent strain. It excessive force is applied to the printed circuit boards, this will result in incorrect operation. Therefore, mount the base unit on a flat surface.

(4) Avoid mounting the base unit close to vibration source, such as large-sized magnetic contactors and no-fuse breakers, install the base unit in another panel or separate the base unit from the vibration source.

(5) Provide a wiring duct as necessary.
However, if the dimensions from the top and bottom of the PC are less than those shown in Fig. 4.3, note the following points:

(a) When the duct is located above the PC, the hight of the duct should be 50 mm (1.97 in.) or less to allow for sufficient ventilation.

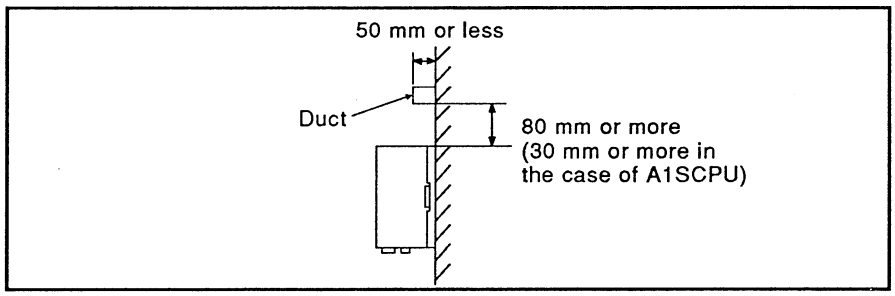


Fig. 4.2 Duct Measurement

Set the distance from the top of the PC so that the hook latch at the top of the module can be pushed. If the hook latch at the top of the module cannot be pushed, the module cannot be replaced.

(b) When the duct is located under the PC, install the duct so that optical fiber cables or coaxial cables may be connected and also consider the minimum bending radius of the cable.

(6) All other equipment should be installed at least 100 mm (3.94 in.) away from the PC to protect it from heat and noise.

(7) The bases must be installed at least 50 mm (2 in.) away from any equipment on both sides.

4.2.2 Installating the A0J2, A0J2HCPU

This section describes the installation of the module.

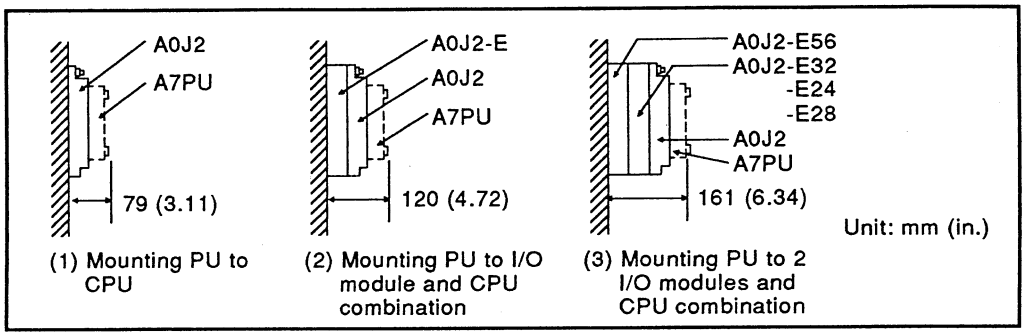


Fig. 4.3 Dimensions in Module-to Module Mounting

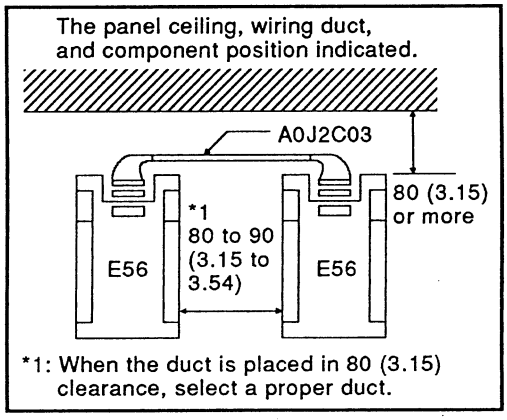


Fig. 4.4 Side-to-Side Installation

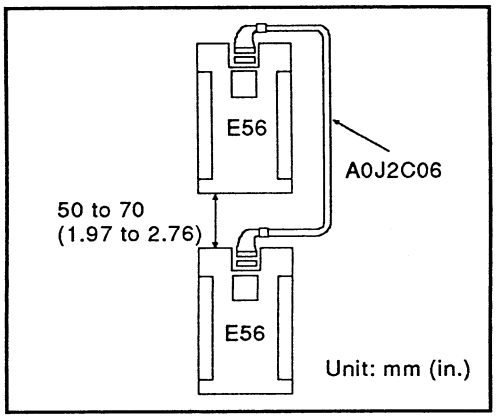


Fig. 4.5 Top to Bottom Installation

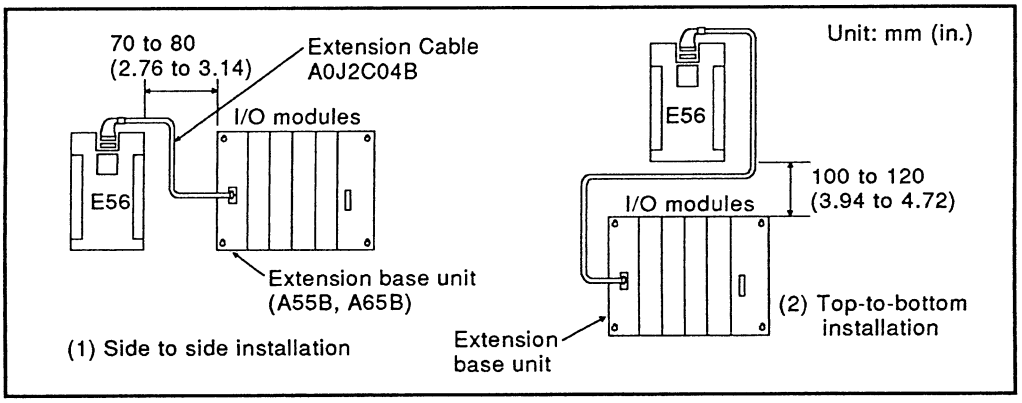


Fig. 4.6 Installation of Extension Base Unit

Fig. 4.7 Horizontal Installation (not allowed)

POINT

The distance from the CPU module front to the external device should be 100 mm (3.94 in.) or more.

4.2.3 Installation The A2CCPU

This section gives conditions for installing the A2C to panel.

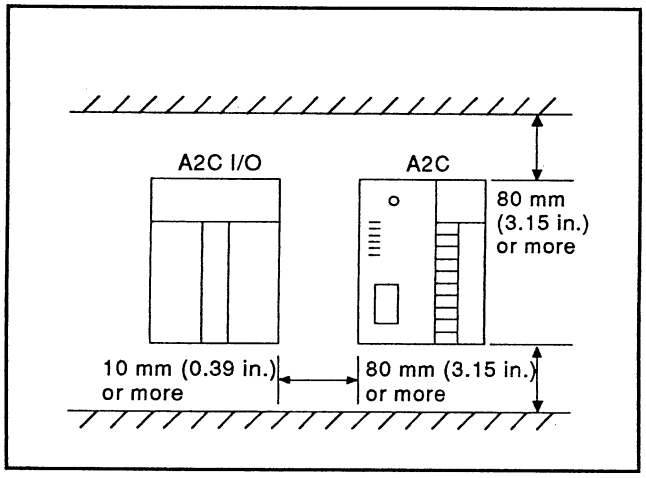


Fig. 4.8 Installing Position

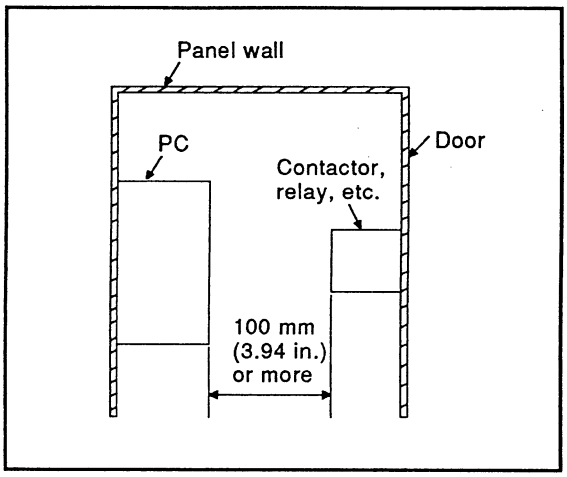


Fig. 4.9 Clearance between PC and Other Devices

4.2.4 Installation The A1SCPU

This section explains the mounting for main and extension base units.

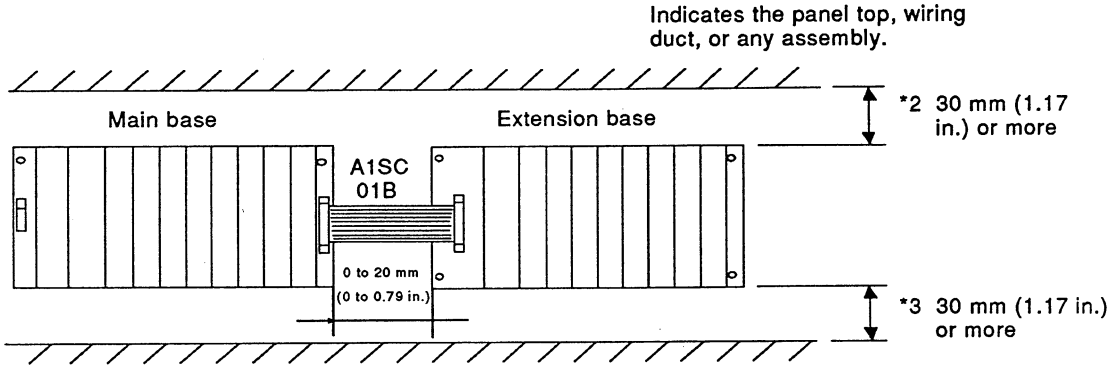
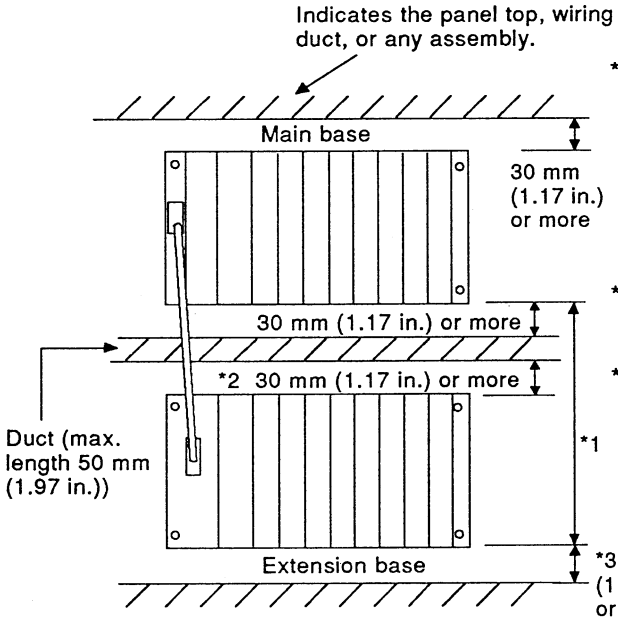


Fig. 4.10 Parallel Mounting



*1: Depends on the length of the extension cable as indicated below.

280 mm (11 in.) or less for A1SC03B cable
1100 mm (43.34 in.) or less for A1SC12B cable
2900 mm (114 in.) or less for A1SC30B cable
350 mm (13.79 in.) or less for A1SC05NB cable

*2: 80 mm (3.15 in.) or more if an A55B, A58B, A65, B or A68B extension cable is used.

*3: 50 mm (1.97 in.) or more if an A55B, A58B, A65B, or A68B extension cable is used.

Fig. 4.11 Serial Mounting

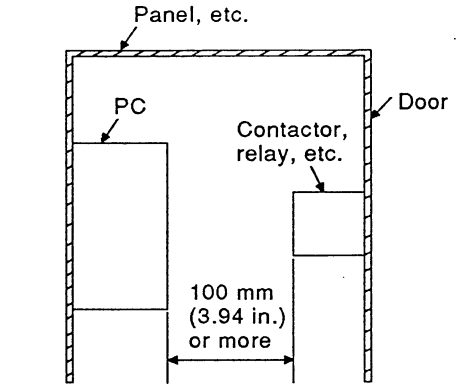


Fig. 4.12 Minimum Front Clearance with Panel Door

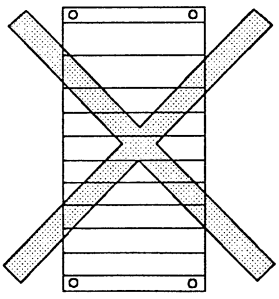


Fig. 4.13 Vertical Mounting (Not allowed)

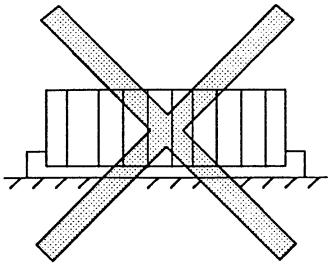


Fig. 4.14 Horizontal Mounting (Not allowed)

4.2.5 Installation the A1, A2 and A3 type CPUs

This section explains the mounting for basic and extension base units.

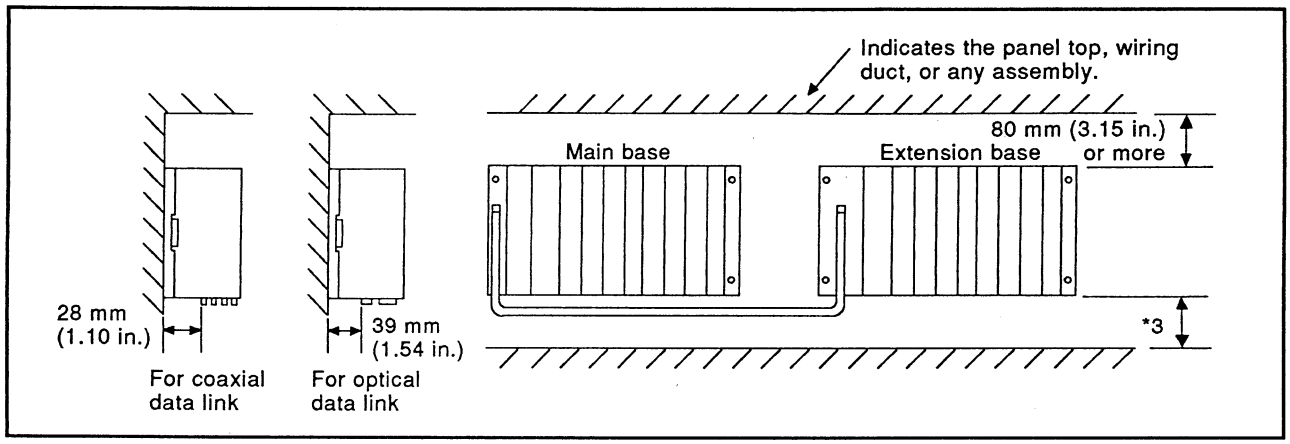


Fig. 4.15 Parallel Mounting

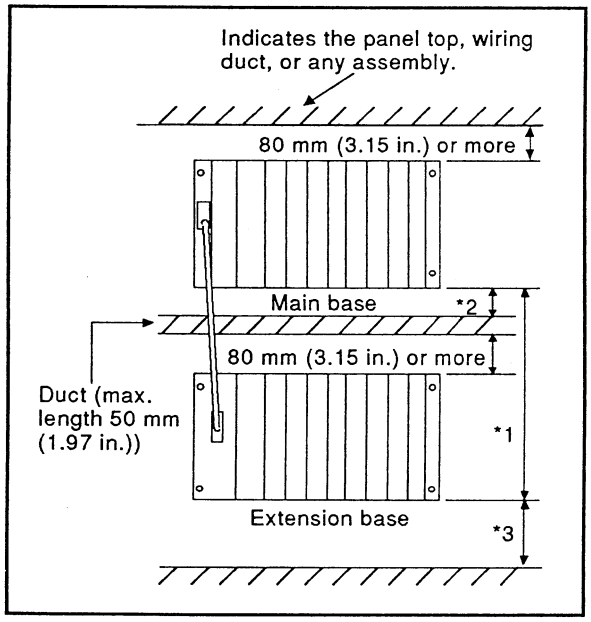


Fig. 4.16 Serial Mounting

*1: Depends on the length of the extension cable as indicated below.

450 mm (17.72 in.) or less for AC06B cable
1050 mm (41.34 in.) or less for AC12B cable
2850 mm (112.21 in.) or less for AC30B cable

*2: 50 mm (1.97 in.) or more when the link unit is not used.
100 mm (3.97 in.) or more when 4.5 mm (0.18 in.) dia. optical fiber cable or coaxial cable is used.
130 mm (5.19 in.) or more when 8.5 mm (0.33 in.) optical fiber cable is used.

*3: 50 mm (1.97 in.) or more when the link unit is not used.
100 mm (3.94 in.) or more when 4.5 mm (0.18 in.) dia. optical fiber cable or caxial cable is used.
130 mm (5.19 in.) or more when 8.5 mm (0.33 in.) optical fiber cable is used.

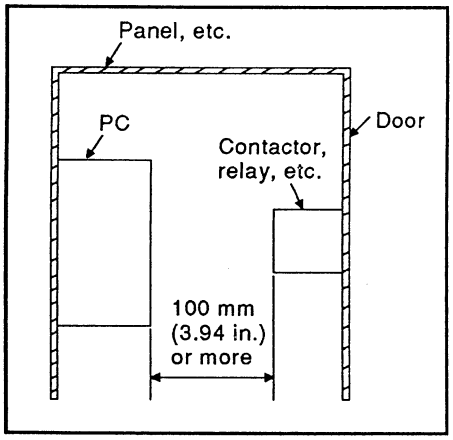


Fig. 4.17 Minimum Front Clearance with Panel Door

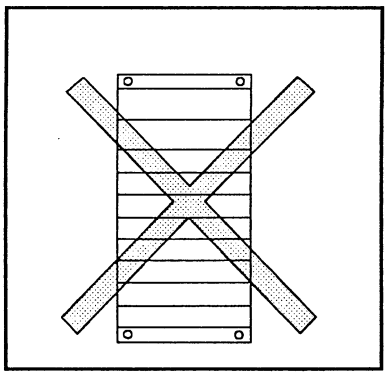


Fig. 4.18 Vertical Mounting (Not allowed)

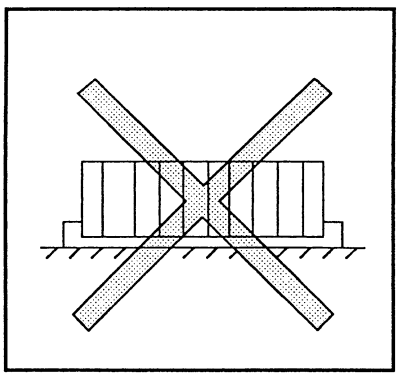
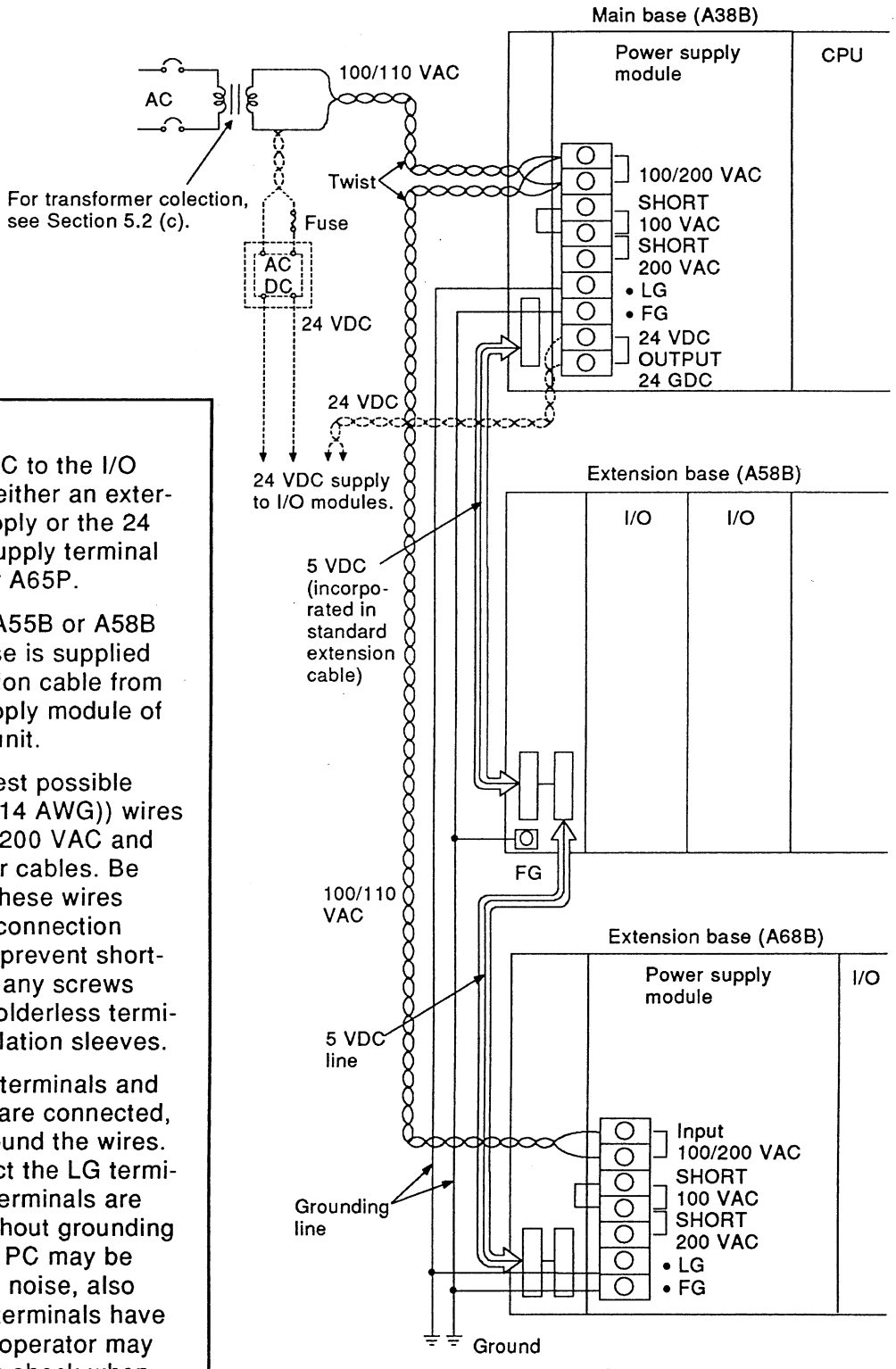


Fig. 4.19 Horizontal Mounting (Not allowed)

5. WIRING AND GROUNDING

5.1 Wiring to Base Units

This section explains the witing of power lines and grounding lines to the main and extension bases.



Flig. 5.1 Wiring and grounding

POINTS

(1) Supply 24 VDC to the I/O module from either an external power supply or the 24 VDC power supply terminal of an A62P or A65P.

(2) 5 VDC to an A55B or A58B extension base is supplied via an extension cable from the power supply module of a main base unit.

(3) Use the thickest possible (max. 2mm^2 (14 AWG)) wires for the 100 V/200 VAC and 24 VDC power cables. Be sure to twist these wires strting at the connection terminals. To prevent short-circuit should any screws loosen, use solderless terminals with insulation sleeves.

(4) When the LG terminals and FG terminals are connected, be sure to ground the wires. Do not connect the LG terminals and FG terminals are connected without grounding the wires, the PC may be susceptible to noise, also since the LG terminals have potential, the operator may get an electric shock when touching metal parts.

5.2 Wiring Instructions

Instructions for wiring the power cable or I/O cables.

(1) Wiring of power source

(a) When voltage fluctuations are larger than the specified value, connect a constant-voltage transformer.
However, use a constant-voltage transformer whose output waveform distortion factor is within 5 %.
Use a constant-voltage transformer for an electronic device and select 2 to 3 times the capacity shown in (c).

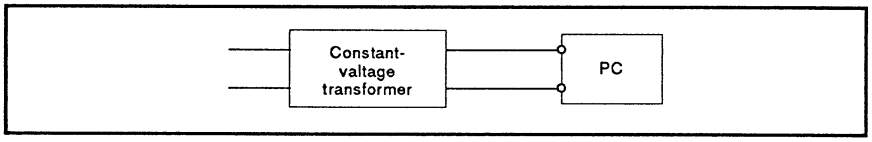


Fig. 5.2 Constant-voltage transformer

(b) Use a power supply which generates minimal noise across wire and across PC and ground. When excessive noise is generated, connect an insulating transformer.

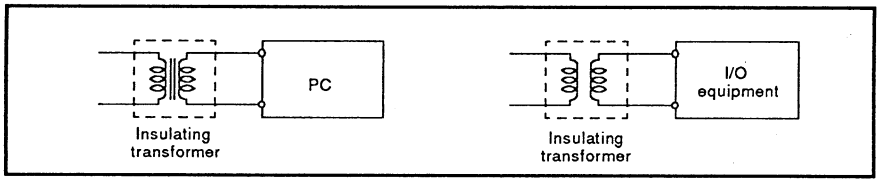


Fig. 5.2 Constant-voltage transformer

(c) When power transformer or insulating transformer is employed to reduce the voltage from 200 VAC to 100 VAC, use one with a capacity greater than that indicated in the following table.

Power Supply Module	Transformer Capacity
A0J2CPU built-in A0J2HCPU built-in	56 VA
A0J2PW	120 VA
A2CCPU built-in A66PC	110 VA
A1S61P A1S62P	110 VA
A1CPU built-in A1NCPU built-in	110 VA
A61P A62P A65P	110 VA

Use a constant-voltage transformer that has 2 to 3 times the above capacities taking into consideration the rush current to the power supply module.

(d) When wiring, separate the PC power source from those for I/O equipment and power equipment as shown below.

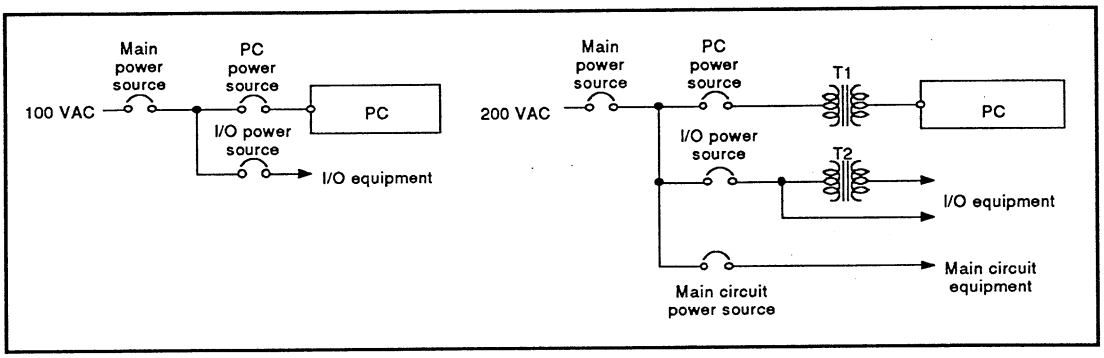


Fig. 5.4 Wiring system

(e) Twist the 100 VAC, 200 VAC, and 24 VDC cables as closely as possible. Connect modules with the shortest possible wire lengths.

(f) To minimize voltage drop, use the thickest (max. 2mm^2 (14 AWG)) wires possible for the 100 VAC, 200 VAC, and 24 VDC cables.

(g) Do not bundle the 100 VAC and 24 VDC cables with main-circuit wires or the I/O signal wires (high-voltage, large current). Also, do not wire the above indicated cables close to the aforementioned wires. If possible, provide more than 100 mm (3.94 in.) distance between the cables and wires.

(h) As a measure against verylarge surges (e.g. due to lightening), connect a surge absorber as shown below.

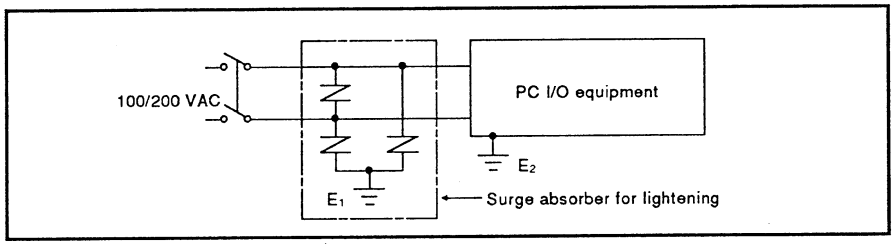


Fig. 5.5 Surege absorber for lightening

POINTS

(1) Ground the surge absorber (E_1) and the PC (E_2) separately from each other.

(2) Select a surge absorber making allowances for power voltage rises.

(2) Wiring of I/O equipment

(a) Applicable size of wire to the terminal block connector is 0.75 (18) to 2 mm^2 (14 AWG). However, it is recommended to use wires of 0.75 mm^2 (18 AWG) for convenience.

(b) Separate the input and output lines.

(c) I/O signal wires must be at least 100 mm (3.94 in.) away from high-voltage and large-current main circuit wires.

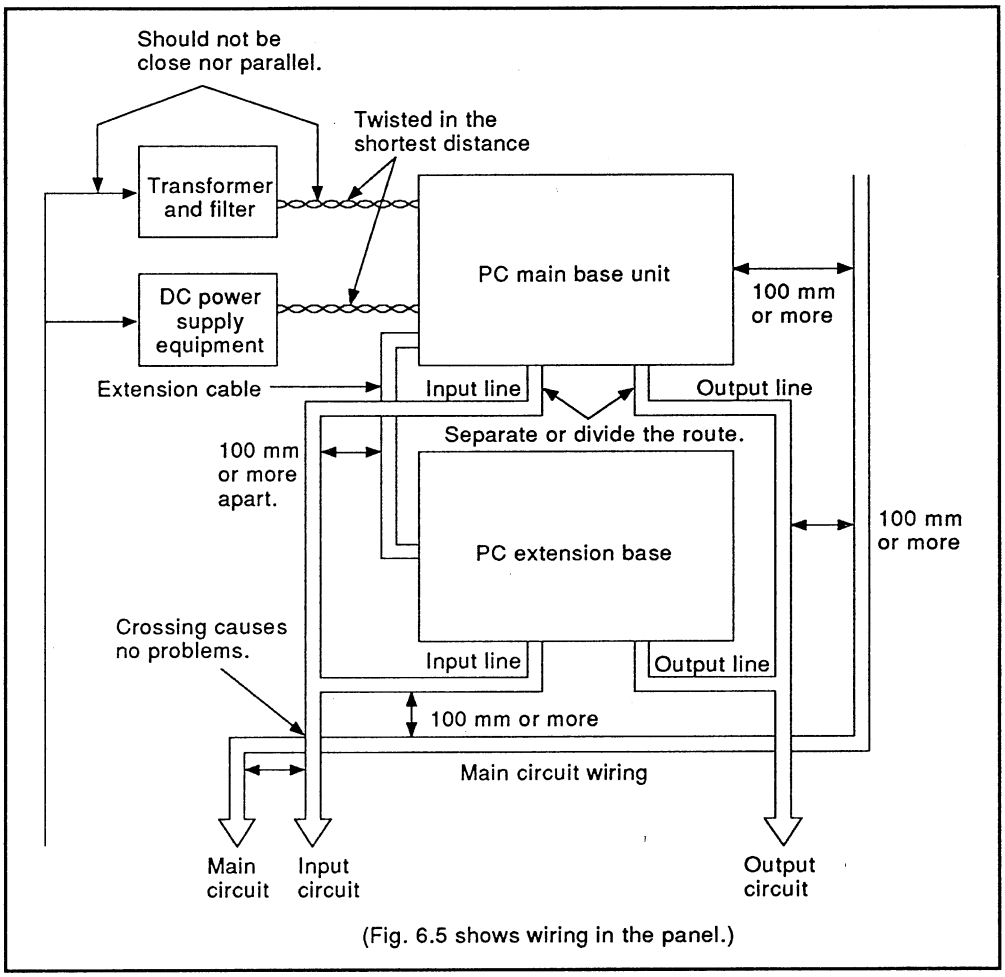


Fig. 5.6 Wiring in the panel

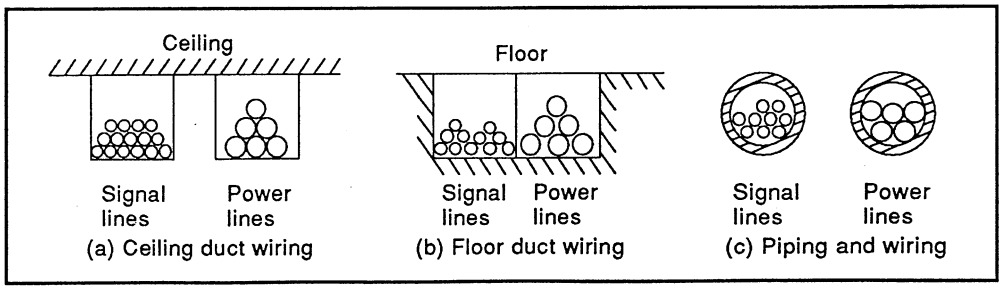


Fig. 5.7 External Wiring

(d) When the I/O signal wires cannot be separated from the main circuit wires and power wires, ground on the PC side with batch-shielded cables. Under some conditions it may be preferable to ground on the other side.

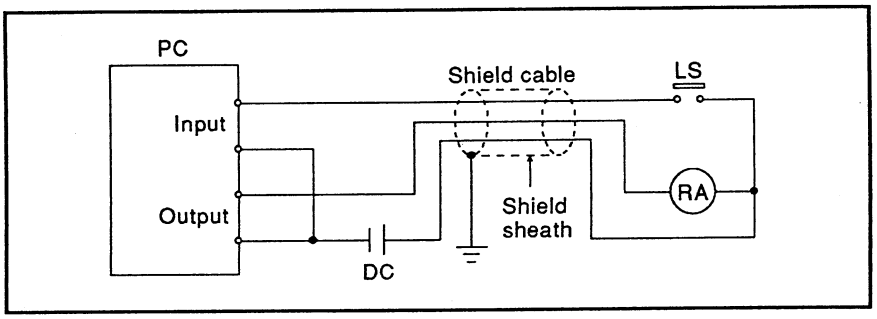


Fig. 5.8 Shielded cable grounding

(e) If wiring has been done with of piping, ground the piping.

(f) Separate the 24 VDC I/O cables from the 100 VAC and 200 VAC cables.

(g) If wiring over 200 mm (7.87 in.) or longer distance, trouble can be caused by leakage currents due to line capacity.

5.3 Grounding

Effective grounding prevents common mode noise.

(1) The A series PC has good noise resistance. Therefore, the PC may be used without grounding except when there is excessive noise. However, follow (b) to (e) described below.

(2) Ground the PC as independently as possible. Class 3 grounding should be used (grounding resistance 100 Ω or less).

(3) When independent grounding is impossible, use the joint grounding method as shown in the figure below (2).

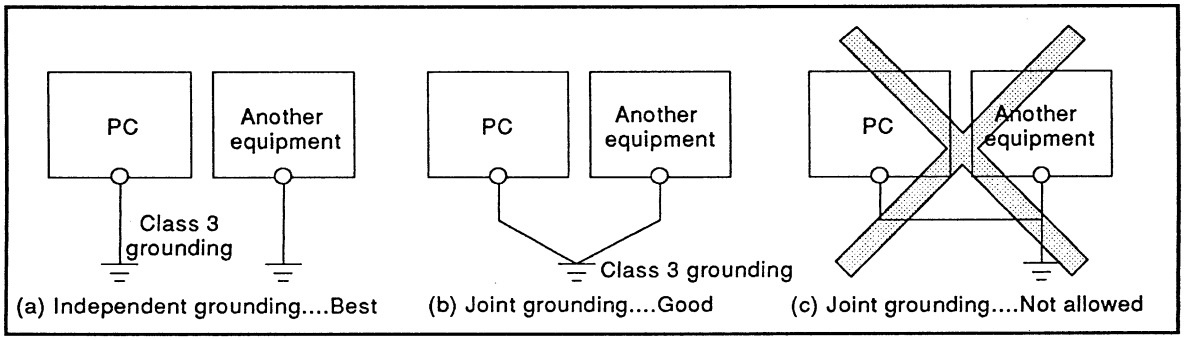


Fig. 5.9 Grounding

(4) Use 2mm^2 (14 AWG) or thicker grounding wire. Grounding point should be as near as possible to the PC to minimize the distance of grounding cable.

(5) Should incorrect operation occur due to grounding, disconnect one or both of the LG and FG terminals of base units from the grounding (See Fig.5.10).
In the case of not grounding, the LG and FG terminals shoud be disconnected.

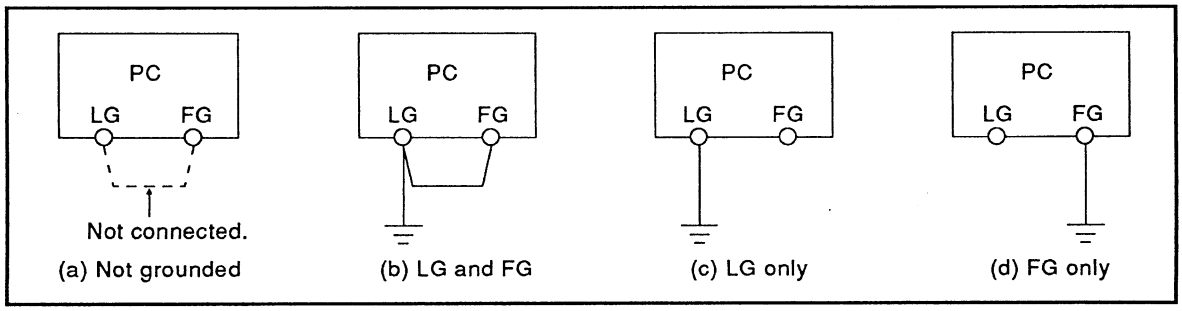


Fig. 5.10 Grounding Terminals

(6) When connecting 200 V (ground voltage: 150 V or more) to the PC power supply or I/O circuit, it is necessary to ground the base metal part from the standpoint of safety (Power supply grounding).

(7) If the PC is not grounded, be sure to ground the panel to prevent stray current (Power supply grounding).

REMARK

LG ..... Ground terminal of the built-in AC power filter
FG ..... Ground terminal of the noise filter of the 5 V, 24 V power supply of the CPU, I/O module, etc.
Also connected with a base shielded pattern.
SG ..... 5 V power supply ground of a CPU, I/O module, etc.

6. COUNTERMEASURES AGAINST NOISE

6.1 Common Mode Noise and Normal Mode Noise

(1) Common mode noise

Fig. 6.1 gives the basic idea of common mode noise.

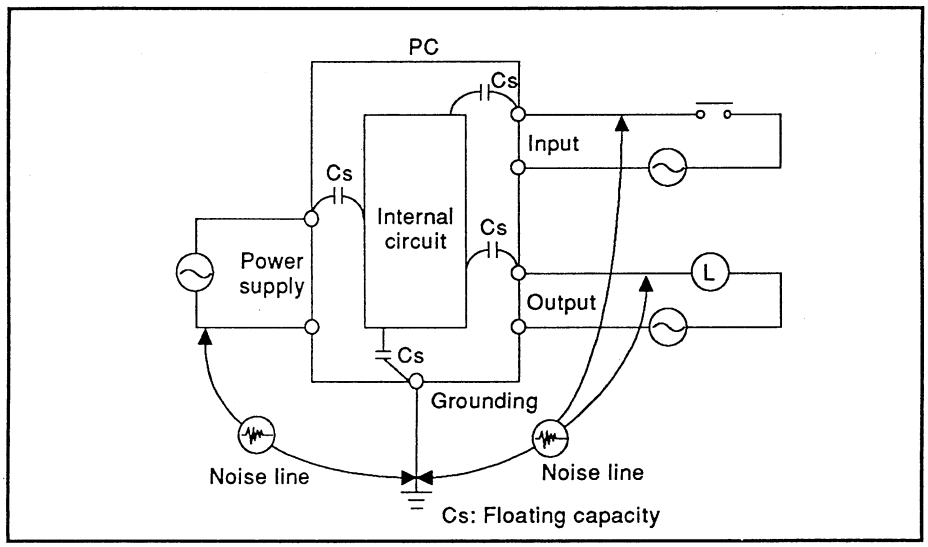


Fig. 6.1 Common Mode Noise

An electric potential difference is generated by noise between the ground, the power supply, and the I/O signal line, and the internal circuit is disturbed, which causes a malfunction. This is called common mode noise.
Charging and discharging of electrical charges arises by the floating capacity between each external signal and the internal circuit, which causes the internal circuit voltage to fluctuate suddenly. This generates common mode noise.
Common mode noise is explained by the following phenomenon:
If a glass filled with water is moved rapidly, the water becomes agitated. This occurs because of the potential difference between the glass and the water.
Normal mode noise is equivalent to the agitation of the water in the glass, but is not the difference between the potential of the glass and the potential of the water.
Common mode noise generally has a greater effect on a PC than normal mode noise. However, because normal mode noise is line noise, it can be removed by a filter. On the other hand, since common mode noise is related to the floating capacity, it cannot be removed easily.
The user can take countermeasures for normal mode noise. However, the user cannot take effective countermeasures for a PC because the manufacturer determines the common mode noise resistance.
The strength for a common mode noise is determined by using the floating capacity Cs. If the PC has a metal case, common mode noise is generally weak. Grounding is an important countermeasure for common mode noise.
Common mode noise occurs by noise induced from other lines to the line, high voltage inductive voltage, radio waves, and static electricity.

(2) Normal mode noise

Figure 6.2 gives the basic idea of normal mode noise.

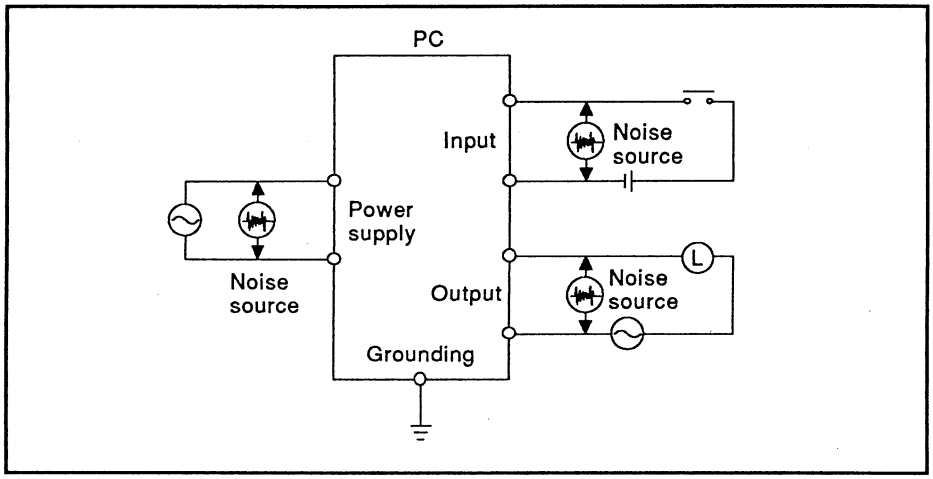


Fig. 6.2 Normal Mode Noise

As shown in the figure, normal mode noise applies to input, output, and power supply lines. Thus, it is sometimes called line noise.
Most normal mode noises are caused by the counter electromotive force of an inductive load connected to the line. Noise that occurs in a device connected to a power supply system appears in the power supply circuit. Noise that occurs in a device controlled by a PC appears in an output line.
Normal mode noise can be prevented by doing noise suppression in the device where the noise is generated and by installing a filter, a transformer, and a surge suppressor in the PC.

6.2 Power Supply

(1) Power supply noise

When a noise occurs frequently in the load that drives other electric power devices and the PC, one effective countermeasure is to insert a shielded transformer or filter as shown in the following figure. Connect the noiseless power supply line that comes out from the transformer or a filter to the PC using the shortest possible distance. In this case, do not bundle the power supply line with other lines, and make sure they do not intertwine.

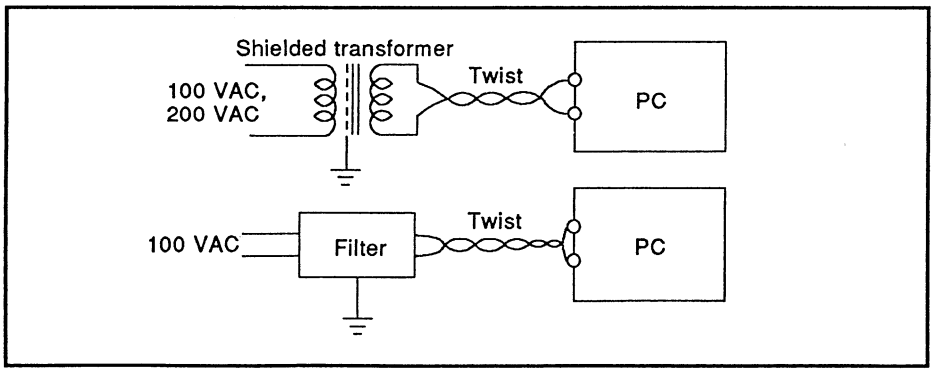


Fig. 6.3 When Power Supply Noise Occurs Frequently

(2) Power supply connection

100 VAC, 200 VAC, and 24 VDC power supply lines connected to a PC should be at least 2 mm^2 thick. Connect after twisting them as closely as possible.
Ensure that the primary side and the secondary side wiring of the transformer, etc. are not parallel; make sure they are at least 100 mm apart.

(3) Power supply system

Separate the PC and I/O device power supplies at the breaker. Mitsubishi recommends separating the wiring routes (See Fig. 5.3).

6.3 Grounding

Grounding of the PC ground terminal has the effect of decreasing the noise (common mode noise) between the power supply, I/O lines, and the main body.
Section 5.4 gives details.

6.4 PC Panels

(1) Arrangement of modules

As shown below, PC I/O modules should be arranged next to the CPU as shown below.
The basic idea is to arrange modules to keep the CPU as far as possible from noise sources. Arrange the modules from the CPU in the following order:

- Special-function module
- DC input module
- Small current DC output module
- AC input module
- DC output module
- Triac output module
- Contact output module

Arrange modules when allocating I/O before programming.

Power supply module	CPU module	Special-function module	DC input module	Small current DC output module	AC input module	DC output module	Triac output module	Contact output module

Fig. 6.4 Module Arrangement

(2) Panel arrangement

Always pay careful attention to the following when determining where to install the PC:

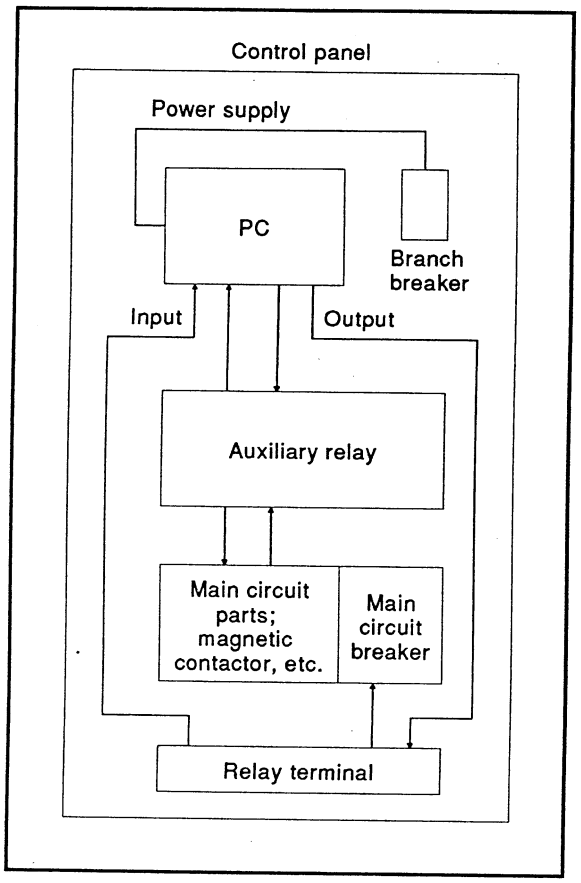


Fig. 6.5 Panel Arrangement

- Separate PCs as far as possible from devices such as magnetic contactors, fuse breakers, etc. that create an arc when switching.
- Separate the PC as far as possible from high voltage and a high current main circuit cable routes.

In addition to countermeasures against noise, the position must also be considered from the standpoint of good ventilation, temperature consistency, minimal vibration and shock, and ease of PC operation and maintenance.

(3) Panel wiring

See Section 5.

6.5 External I/O Signal Wire

- Make every effort to keep the I/O signal wire separate from the main circuit high-voltage, large current cables.
- If separation cannot be done, perform grounding on the PC side by using a batch shielded cable (See Fig. 5.8).
- If external wiring is 200 m or more, or in the case of an AC input signal with a large inductive voltage, use a shielded line at each point, or take appropriate countermeasures as shown in the following figure.
  In the case of long-distance wiring (hundreds of meters), PC input and output lines should be separated.

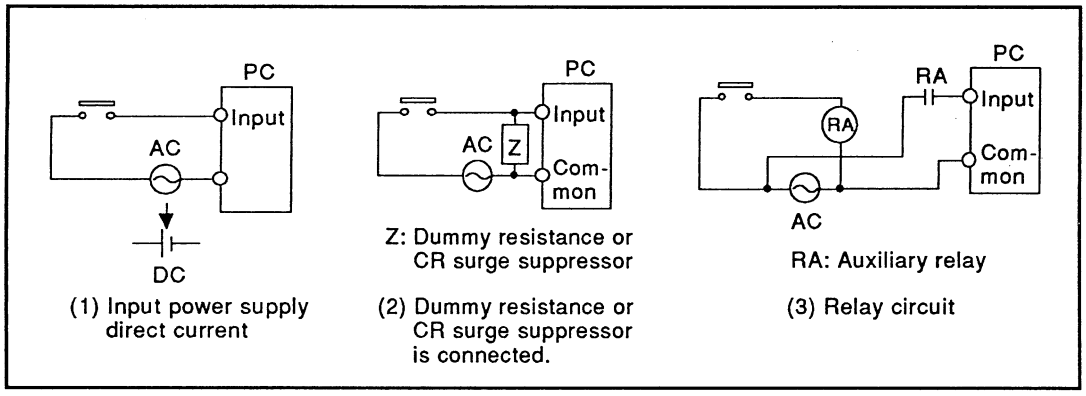


Fig. 6.6 Countermeasures Against Input Inductive Voltage

(1) Input device

1) If the inductive load is connected parallel to the input module of a PC, connect a CR surge suppressor parallel to a load for the AC input as shown below. Connect a fly wheel diode parallel to the DC input load. Connect a surge suppressor as close as possible to the inductive load.

2) If the input device incorporates an operation display neon lamp, or if a limit switch is used as input, voltage is sometimes created by the neon lamp current even when the limit switch contact is open. If this voltage is large, take countermeasures against inductive voltage, as shown in Fig. 6.6 below.

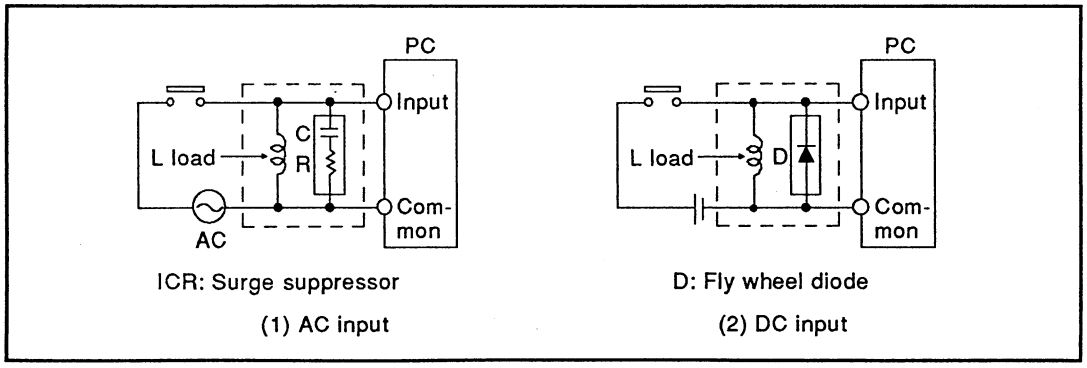


Fig. 6.7 When Inductive Load is Parallel with Input

(2) Output device

In the case of inductive loads, noise is created by rush current when an output signal goes ON. In addition, when an output signal is turned OFF, noise is created by a counter electromotive force. Arc noise is also created from contacts such as magnetic contactors, etc.
If sufficient noise countermeasures have been taken on the PC side, it is not necessary to take special countermeasures. Take the following countermeasures when improving noise intensity or reducing influences on other electronic devices:

1) In the case of AC inductive load, connect CR surge suppressors to both ends of the load. Use a CR surge suppressor of 0.5 μF + 47 Ω for 100 VAC, 200 VAC, and 400 VA. If this CR surge suppressor is not connected to the position closest to the load, it will have no effect (See Fig. 6.8).

2) In the case of DC inductive load, connect fly wheel diodes to both ends of the load. Connect these diodes closest to the load. The opposite withstanding diode voltage must be at least four times that of the load voltage (See Fig. 6.9).
When a fly wheel diode is connected to a DC inductive load, the load operation is delayed by the current flowing in the diode during breaking. If this delay causes a problem, connect a CR surge suppressor, in addition to taking the abovementioned countermeasures against AC inductive load noise.

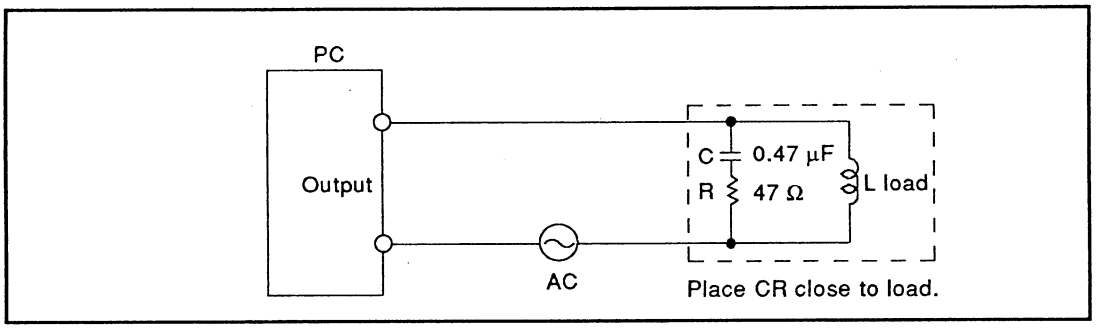


Fig. 6.8 Countermeasures Against AC Induction Load Noise

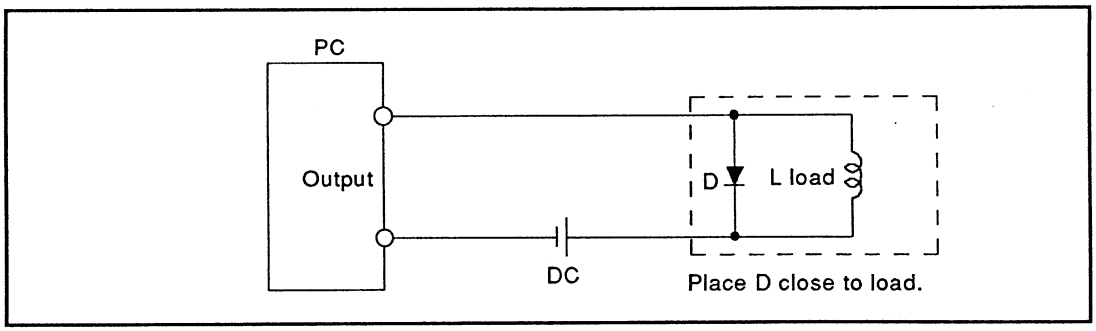


Fig. 6.9 Countermeasures Against DC Inductive Load Noise

3) When the load to be connected to a PC output is opened and shut at the external contact, be sure to take the same countermeasures in Figs. 6.8 and 6.9, regardless of the presence or absence of noise countermeasures on the PC side (See Fig. 6.10).

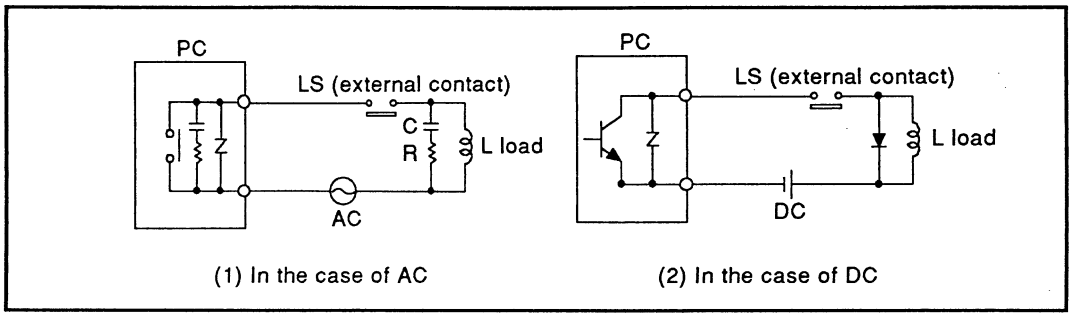


Fig. 6.10 When Opening and Shutting a Load at the External Contact

4) Switching by using a triac that breaks when the load current is zero is effective for an AC inductive load with significant noise during breaking.

5) Connecting CR surge suppressors to both ends of the contact is effective as a countermeasures against arc noise during contact switching of magnetic contactors. Be alert for leakage current by the CR surge suppressor circuit even when the contact is open (See (A) in Fig. 6.11).

6) If the break noise of the motor and transformer create problems, connect a CR surge suppressor between the phases (See (B) in Fig. 6.11).

7) The relay in the panel has also an effect (See Fig. 6.12).

The basic idea behind the anti-noise countermeasures of a solenoidal device is to repress the noise-generating source. Items 1) to 6) above corresponds to this. Take the countermeasures given above for a PC output with a large noise occurrence. When connecting a device with weak noise, select the output module of a PC with a surge suppressor. Use the contact output module without a surge suppressor only for an electronic timer, motor-driven timer, miniature relay, or a lamp.

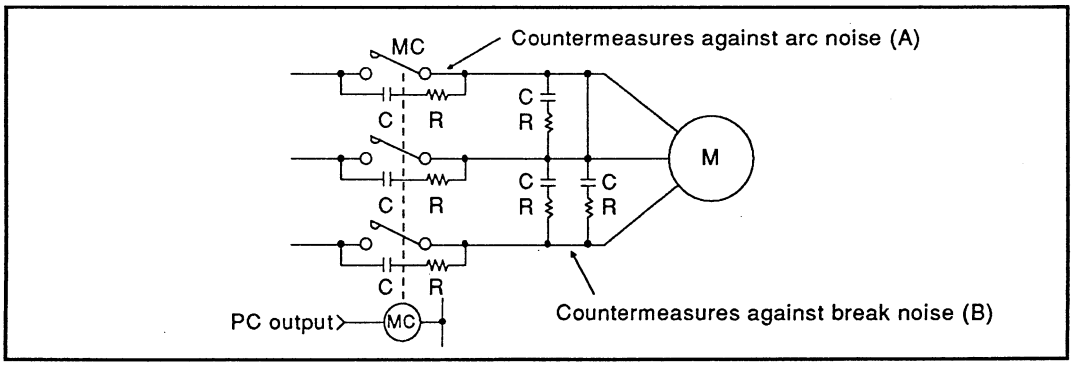


Fig. 6.11 Countermeasures Against Large-Capacity Load Noise

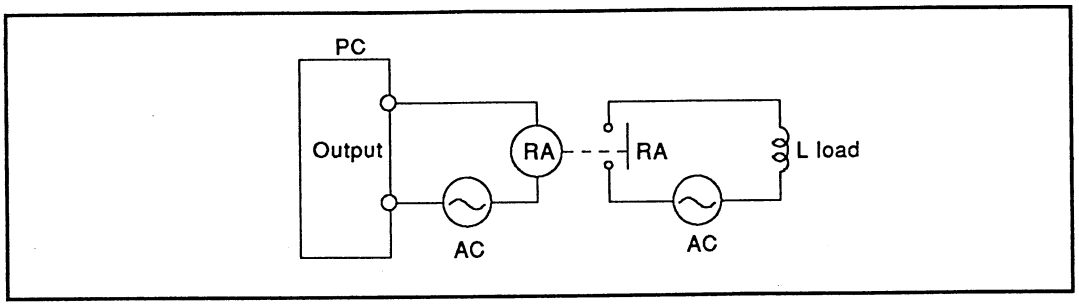


Fig. 6.12 Load Driving by Using Relays

6.6 Troubleshooting and Noise Countermeasures

When one of the following control errors occur, external noise is considered to be the cause.

(1) When an error occurs which synchronizes with the operation of a specific output device controlled by the PC

In this case, noise or a surge from the output device are usually considered to be the cause.
When a device is turned ON and OFF, an error may occur, stopping the PC. Take the anti-noise countermeasures explained under "Output device" earlier in this section. The countermeasures given in Figs. 6.8 and 6.9 are normally effective. If a surge suppressor and a diode are not installed in the position closest to the load, it will have no effect. In the case of a mass load, take the countermeasures given in Fig. 6.11.
Faulty connections, such as a slack input line, disconnections, faulty ground contacts, mixed contacts and input devices, etc. are considered as causes of problems that occur which synchronize with the operation of other devices. Therefore, check them very carefully.

(2) When an error occurs which synchronizes with the operation of other devices that do not relate to the PC

In such cases, the cause is noise or surge from another device. Take the same countermeasures as those for (1) above for the corresponding device.
If these countermeasures do not solve the problem, ground any devices which are not grounded. When they are grounded, try ungrounding them. Separate I/O signal lines from the wiring of a correspondent device. Or, change the route.

(3) When an error occurs when a large-capacity load is turned ON

Power supply voltage drop and the rise of the ground electric potential of a shared ground are considered as causes.
When the power supply voltage drops below the specified value when it is turned ON, change the power supply system by installing a low voltage transformer in the power supply.
When grounded, try ungrounding.

(4) When the operation of the PC is randomly unsteady

Although most causes for such PC problems are given in (1) to (3) above, other factors could include the following:

1) Frequent momentary power supply failures. Or particularly bad waveforms.
2) When there is a great deal of voltage noise
In such cases install a constant-voltage transformer, or change the power supply system. Also, using only an insulation transformer can be effective.
3) Influence of high-frequency equipment
Grounding high-frequency equipment and the PC panel. The I/O signal line of a PC should be shielded.

(5) When an inductive voltage of the input is large

In this case, the PC does not stop and an output error occurs cause by erroneous input. Even if the inductive voltage is low, a wrong input occurs by noise.
In this case, take the countermeasures given in Fig. 6.6.

Take the above countermeasures against PC noise problems. When making a panel, or when constructing external wiring, costs can be reduced by taking these countermeasures. When setting a system using a PC, it is important to consider which countermeasure should be taken.
It is also necessary to check whether the countermeasures taken when the problem occurred were really effective by removing the countermeasures in order to reproduce the problem.

7. TEST OPERATION AND ADJUSTING

7.1 Check Points Before Start of Test Operation

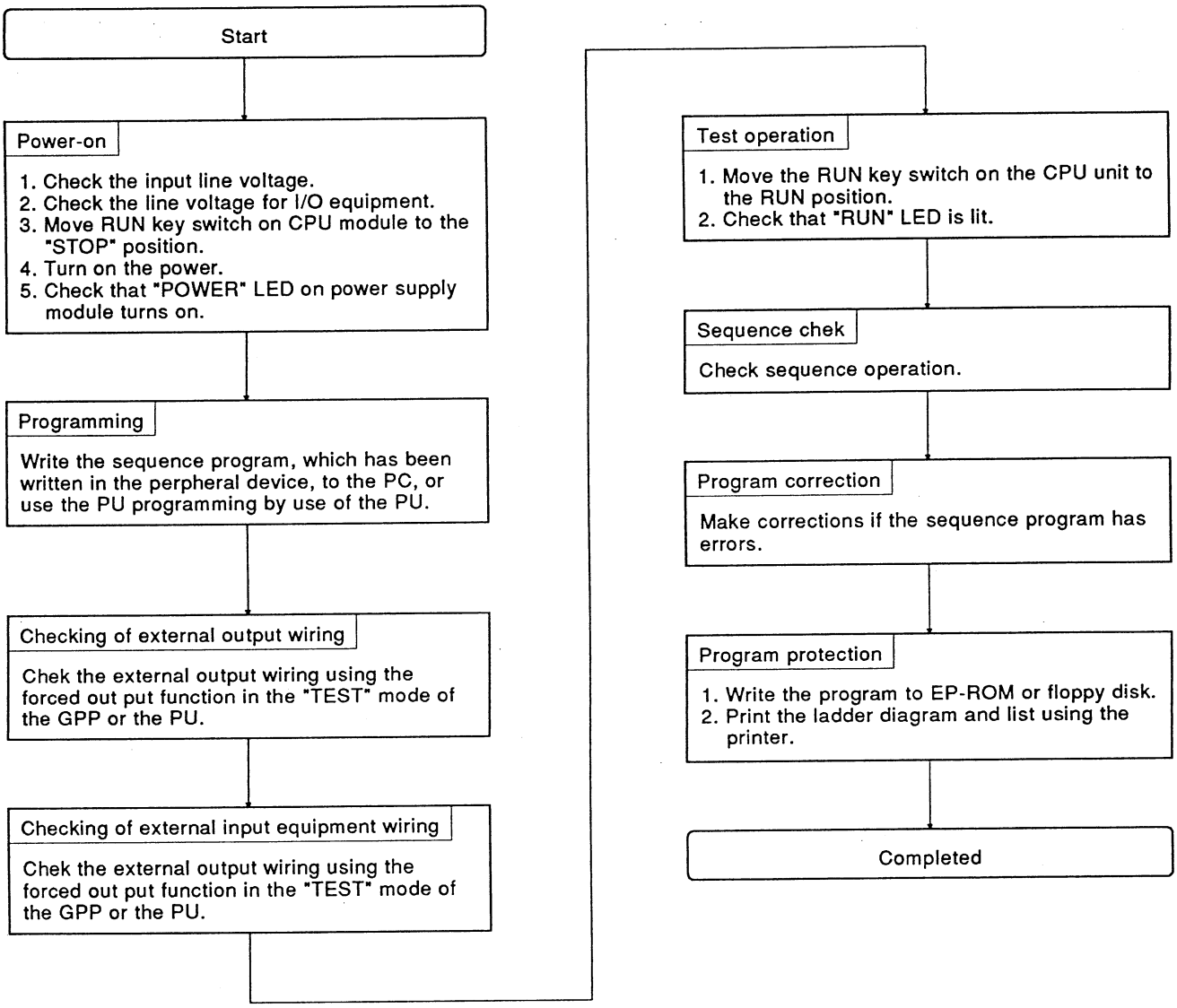
This section expains the points to be checed prior to the test operation of programmable controller.

Tabel 7.1 Check Points

Item	Check Point	Description
1	Loading and setting of memory cassette	1) Check that the memory cassette is securely inserted into the CPU module. Check that the memory cassette clicks when loaded. 2) Check that the used memory capacity matches the capacity of the memory cassette. 3) Check that the RAM/ROM setting is correct. 4) Check that the RAM or ROM is loaded securely. 5) Check that the memory protect is ON.
2	Loading of battery (inside the memory cassette)	1) Check whether the connector for battery lead wires, which has been disconnected before shipment, is securely inserted in the pin connector on the printed circuit board. (The red lead is positive and the blue lead negative.) 2) Check that the voltage of battery has not reduced. (Nominal value: 3.6 V)
3	Connection of extension cable	1) Check that the connectors of main base and extension base are properly connected with the connectors of extension cable. 2) Check that the connector position of extension base is correct.
4	Extension stage number setting of extension base	1) Check that setting has been performed. 2) Check that the same number has been set. 3) Check whether one base has been set at more than one place.
5	Loading of modules	1) Check that the types of unit loaded in each slot of main base and extension base is correct. 2) Check that the setting of the point setting switch of dummy unit (AG62) is proper. 3) Check whether the module configuration uses more I/O points more than the I/O points of CPU specificaions.
6	Fuse	1) Check if the fuse has blown or been damaged.
7	Connection of power and I/O cables	1) Check the cables connected to each terminal of the terminal block. 2) Check the terminal screws of terminal block for the power supply module and terminal block for I/O module. 3) Check the cable size.

7.2 Test Operation and Adjusting Procedure

This section shows the flow chart from after the completion of installation to the test operation of programmable controller.



8. MAINTENANCE

8.1 Malfunction Analysis

The PC is designed so that if a malfunction occurs in any of its modules, that module will be replaced, not repaired. The pie charts below show the results of a questionnaire prepared by NECA (Nippon Electric Controller Association). They show the malfunction location, malfunction cause, and malfunction stop time percentages when problems occur with a PC.

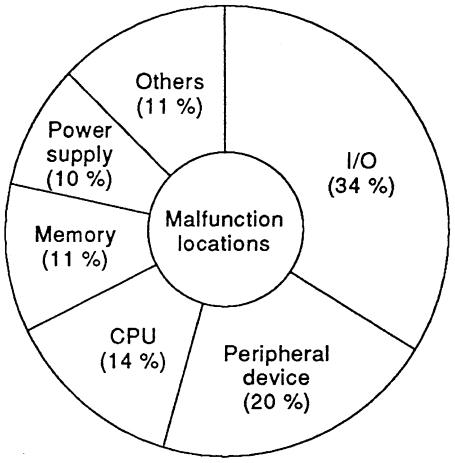


Fig. 8.1 Malfunction Location Percentages

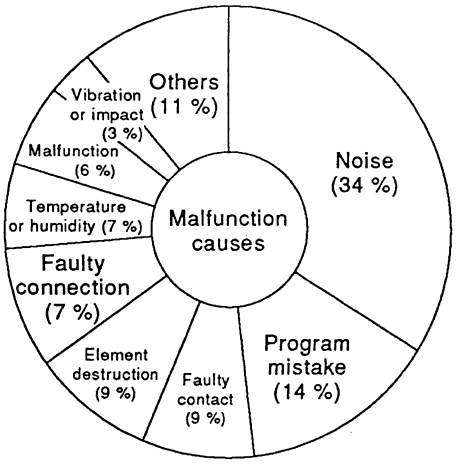


Fig. 8.2 Malfunction Cause Percentages

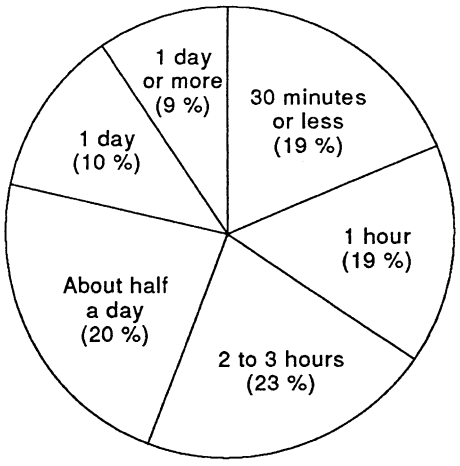


Fig. 8.3 Malfunction Stop Time Percentages

8.2 Maintenance

To ensure the PC is in the best operating condition, perform the following checks daily or periodically:

(1) Daily inspection

Table 8.1 shown the inspection items which are to be checked daily.

Table 8.1 Daily Inspection

No.	Check Item		Check Point	Judgement	Corrective Action
1	Base unit mounting conditions		Check loose mounting screws and cover.	The base unit should be securely mounted.	Retighten screws.
2	Mounting conditions of I/O module, etc.		Check if the module is desengaged or the hook is securely engaged.	The hook shoud be securely engaged and the module should be positively mounted.	Securely engage the hook.
3	Connecting conditions		Check for loose terminal screws.	Screws should not be loose.	Retighten terminal screws.
			Check distance between solderless terminals.	Proper clearance should be provided between solderless terminals.	Correct.
			Check connectors of extension cable.	Connections should not be loose.	Retighten connector mounting screws.
4	CPU module indicator lamps	"POWER" LED	Check that the LED is on.	On. (Off indicates an error.)	• Power supply and voltage check • Fuse check • Power supply module installation
		"RUN" LED	Check that the LED is on during run.	On. (Off or flicker indicates an error.)	Varies according to the type of CPU. See the corresponding manual.
		Input LED	Check that the LED turns on and off.	On when input is on. Off when input is off. (Display, which is not as mentioned above, indicates an error.)	
		Output LED	Check that the LED turns on and off.	On when output is on. Off when output is off. (Display, which is not as mentioned above, indicates an error.)	

(2) Periodic inspection

This section explains the inspection items which are to be checked every six months to one year. If the equipment have been moved or modified or wiring has been changed, also make the inspection.

Table 8.2 Periodic Inspection

No.	Check Item		Check Point	Judgement	Corrective Action
1	Amvient environment	Ambient temperature	Measure with thermometer and hygrometer. Measure corrosive gas.	0 to 55 °C	When PC is used inside a panel, the temperature in the panel is ambient temperature.
		Ambient humidity		10 to 90 %RH	
		Ambience		Ther should be no corrosive gases.	
2	Line voltage check		Measure voltage across 100/200 VAC terminal.	85 to 132 V ---------- 170 to 264 VAC	Change supply power. Change transformer tap.
3	Mounting conditions	Looseness, play	Move the unit.	The module should be mounted securely and positively.	Retighten screws. For CPU, I/O, and power supply modules check all connections
		Ingress of dust or foreign material	Visual check.	There should be no dust or foreign material, in the vicinity of the PC.	Remove and clean.
4	Connecting conditions	Loose terminal screws	Retighten.	Connectores should not be loose.	Retighten.
		Distances between solderless terminals.	Visual check.	Proper clearance should be provided between solderless terminals.	Correct.
		Loose connector	Visual check.	Connectors should not be loose.	Retighten connector mounting screws.
5	Battery		Check battery status by monitoring special auxiliary relays M9006 and M9007. Replace battery if necessary.	Preventive maintenance	If battery capacity reduction is not indicated, change the battery when specified service life is exceeded.
6	Fuse		Check fuses.	Preventive maintenance	Chenge the fuse periodically due to rush current.

8.3 Expendable Items

The expendable items in a PC are the output relays, backup batteries, and fuses.
When an error occurs in the CPU, an I/O module, or power supply module, that module must be replaced.
Batteries and fuses are explained in the following section.

8.4 Output Relay Lifetimes

A contact output module's relay is used up by the make/break switching operation.
When a relay directly attached to the printed circuit board of an output module is used up, the output module must be replaced.

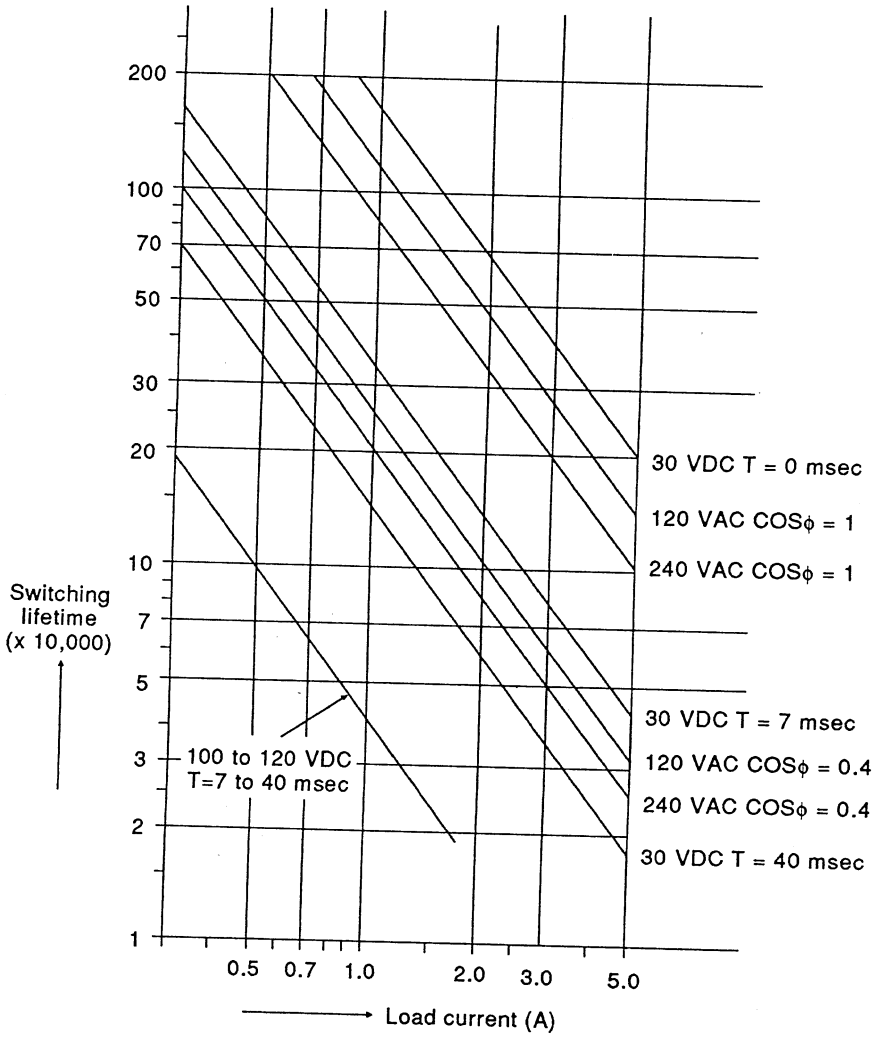


Fig. 8.4 Output Relay Contact Lifetime Characteristics

8.5 Replacement Parts

In Japan, since replacement parts can be easily obtained from service centers, branch offices, agents, etc., they can be purchased as needed. However, when a PC is used overseas, replacement parts must be ordered beforehand.
Pay attention to the following design points. Doing so makes maintenance easier.

(1) Quickly restored types

With building block types, module replacement is easy. Only malfunctioning modules need to be replaced.

(2) Types of memory

IC-RAM memory and latch relay need battery backup.
Since EP-ROM (EEP-ROM) can avoid program changes due to mistakes because batteries are not needed, they are suitable for export.

(3) Reduction of module categories

Desirable for reducing replacement parts categories.

(4) Ensuring replacement contacts

If there are no module replacement parts, the spare number of points can be secured by changing the connection and program (I/O signal change) by not utilizing 10 to 20 % of the 16-point, 32-point, and 64-point I/O modules.

(5) Document creation

Since it is easy to change programs with a PC, operating programs and documents (ladder diagrams, program lists, etc.) may not always correspond. Always prepare the most recent document. A printer is useful for doing so.

(6) Proficiency in handling peripheral devices

Proficiency in handling equipment such as a GPP, HGP, PHP, PU, a printer, etc. can shorten the recovery time when an accident occurs.

(7) Replacement parts

Table 8.3 Replacement Parts

No.	Product Names	Quantities	Remarks
1	Batteries	1 to 2	The storage lifetime of a lithium battery is about 5 years. However, prepare 1 or 2 batteries for unforeseen contingencies. Section 9.1 gives details about specifications.
2	Fuses	Number needed	The AC battery and the output module each have one fuse attached. A fuse can be blown by rush current for many reasons; short circuits, excess current during power ON/OFF, etc. Therefore, always make sure to have enough fuses on hand. Section 9.2 gives details about specifications.
3	Floppy disks	As necessary	Backup floppy disk of the software package used for start-up and replacements for the user's floppy disks.
4	I/O module	One per type	Remember that malfunctions easily occur during test operations. After extended use, the contacts of relay output modules wear out.
5	CPU module	One per type	Since this is the main part of a PC, if it malfunctions, the system will go down.
6	Memory and memory cassette	One set	
7	Power supply module	One per type	Same as above. Since the parts can attain very high temperatures, if the ambient temperature becomes too high, it could shorten the unit's lifetime.
8	Peripheral devices	As necessary	PUs are useful as GPP, HGP, and PHP replacements.

8.6 Program Storage

Think of a program as you would replacement parts, and store it by using a peripheral device.

(1) EP-ROM memory

Data is stored to the ROM by using a GPP or a ROM writer unit. ROM operation of a CPU can be done in case of an emergency.
Since EP-ROMs are compact with excellent storage capacity, they are convenient to use.

(2) FD

Programs are stored to the user disk by using a GPP, HGP, or PHP. 96 programs max. can be stored in a disk. An FD's capacity is larger than that of a cassette tape, and it takes less time for reading and writing.

(3) Cassette tape

Programs are recorded by a tape recorder using either a PU or cassette interface module. Reading and writing take longer than with an FD and the reliability is slightly inferior.

(4) Hard copy

Programs are printed out by using a printer or ladder creation equipment, and the printout is then stored.

9. BATTERIES AND FUSES

9.1 Battery Lifetimes

(1) Replacement of battery

M9006 or M9007 turns on when the voltage of battery for program backup and power failure compensation reduces.
Even if this special relay turns on, the contents of the program and power failure compensation are not lost immediately.
However, if the ON state is overlooked, the PC contents may be lost.
As a preventative maintenance measure, Mitsubishi recommends early replacements of batteries and fuses.
This section explains standards, battery lifetimes, and gives replacement details.

Battery model name	A6BAT

(2) Service life of battery

This service life of the battery depends on the capacity of the memory. table 9.1 shows service life according to memory.

Table 9.1 Battery Lifetimes

Battery Lifetimes / CPU Model Names/ Memory Cassette Model Names		Battery Lifetimes (Total Power Failure Times) (Hr)	
		Guaranteed Hours	Actual Use Hours
A2 type CPUs A3 type CPUs	A3MCA-0 A3NMCA-0	10800	27000
	A3MCA-2 A3NMCA-2	7200	18000
	A3MCA-4 A3NMCA-4	5400	13000
	A3MCA-8 A3NMCA-8	3600	9000
	A3MCA-12 A3NMCA-16	2150	5400
	A3MCA-18 A3NMCA-24	1950	4900
	A3NMCA-40	1400	3500
	A3NMCA-56	450	1125
	A3AMCA-96	1860	9495
A0J2, A1 type CPUs		7200	18000
A0J2H, A2C, A1SCPU		5400	13000

*The actually applied value indicates a typical value and the guaranteed value indicates the minimum value.

Preventive maintenance is as described below.

1) Even if the total power failure time is less than the guaranteed value in the above table, change the battery after four to five years.
2) When the total power failure time has exceeded the guaranteed value in the above table and M9600 has turned on, change the battery.
   When a power failure occurs, the battery lifetime lasts about one week (168 Hr.) after M9006 goes ON.

(3) Replacement

Although the times between connecting a new battery after disconnection an old battery vary according to the type of memory cassette, all replacements must be done within 3 minutes.

9.2 Fuses

Table 9.2 List of Fuses

Models	Purposes	Modules	Model Names	Ratings	Shapes	Measurements (mm)	Manufacturers
Building block	For power supply	A1 type CPUs A61P, 62P 65P, 66P	GTH4	4A	Glass tube	ϕ 6 x 32	Nagasawa
		A63P	SM6.3A	6.3A	Same as above	ϕ 6 x 32	Same as above
	Output module	AY22	HP-70K	7A	Plug	30.3 x 8 x 20	Daito
		AY23	HP-32	3.2A	Same as above	Same as above	Same as above
		AY50, 80	MP-20	2A	Same as above	17.2 x 5.5 x 19	Same as above
		AY60	MP-32	3.2A	Same as above	Same as above	Same as above
		AY60E	MP-50	5A	Plug	17.2 x 5.5 x 19	Daito
		AY11E, 13E	MF51NM8	8A	Glass tube	ϕ 5.2 x 20	Nagasawa
A0J2	Triac output module	A0J2-E[ ]S	HP-32	3.2A	Plug	30.3 x 8 x 20	Daito

(Note)
Fuses for the power supply of an A0J2, A0J2H, A2C, A1SCPU and the fuse for an A1S output module cannot be interchanged.

MEMO

10. POWER SUPPLY MODULE SELECTION

Select the power supply module in accordance with the total current consumption of each input/output, and the special-function module and a peripheral device for 5 VDC to be supplied by the power supply module.
When an extension base which does not a power supply is used, it is necessary to take into account that it's power must be supplied by the power supply module of the main base unit.
The wiring supply from the 24 VDC output of a power supply module for each input/output and special-function module which require 24 VDC can be used.

10.1 Selecting an Extension Power Supply Module for an A0J2 or A0J2H CPU

(1) 5 VDC current consumption of each module

The output current capacity 5 VDC current consumption and all power supply modules are given below.
Calculate whether an extension power supply module is necessary by using the following chart.

5 VDC current consumption of an A0J2 or A0J2H module (A)

Output current of a power supply module

A0J2, A0J2H CPU built-in 5 VDC 2 A 24 VDC 0.5 A
A0J2PW 5 VDC 2 A 24 VDC 0.5 A
A0J2-DC24 A0J2H-DC24 CPU built-in 5 VDC 2 A
A0J2PW-DC24 A0J2HPW-DC24 5 VDC 2.5 A
A0J2C25 5 VDC 2 A 24 VDC 0.5 A

CPU Types	For Single	For Optical Link	For Coaxial Link
A0J2CPU	0.3	0.52 (P23)	0.96 (R23)
A0J2HCPU	0.4	0.53 (P21)	0.86 (R21)
A0J2HCPU-DC24	0.4	———	———

Input Modules	
A0J2-E32A	0.105
A0J2-E32D	
A0J2E-E32D	

Output Modules	
A0J2-E24R	0.145
A0J2-E24S	0.4
A0J2-E24T	0.145
A0J2E-E24R	
A0J2E-E24T	

I/O Modules	
A0J2-E28AR	0.14
A0J2-E28AS	0.26
A0J2-E28DR	0.13
A0J2-E28DS	0.26
A0J2-E28DT	0.125
A0J2E-E28DR	0.13
A0J2E-E28DS	0.23
A0J2E-E28DT	0.25
A0J2-E56AR	0.225
A0J2-E56AS	0.46
A0J2-E56DR	0.23
A0J2-E56DS	0.46
A0J2-E56DT	0.255
A0J2E-E56DR	0.23
A0J2E-E56DS	0.46
A0J2E-E56DT	0.225

Peripheral Devices	
A7PU	0.4
A7PUS	0.4
A6WU	0.8
AD71TU	0.3
A6GPP	Not consumed.
A6HGP	
A6PHP	
A7PHP	

Special-Function Modules		
A0J2P25	Data link remote I/O	0.47
A0J2R25		0.89
A0J2C25	Multidrop link	0.3
A0J2-D61S1	High-speed counter	0.1
A0J2-68AD	A-D conversion	0.7
A0J2-62DA	D-A conversion	0.55
A0J2-D71	2-axis positioning	0.65
A0J2-C214S1	Computer link	0.3

When the power is supplied from the A0J2HCPU (P21/R21)'s built-in power supply, the total internal current consumption of the entire system should be within A0J2HCPU's built in power supply capacity range.

CPU's built-in power supply capacity: 5 VDC, 2A	>	5 V current consumption of CPU	+	5 V current consumption of simultaneously "ON" I/O modules	+	5 V current consumption of peripheral device (A7PU)
24 VDC, 0.5 A	>	Current consumption of 24 VDC input simultaneously "ON" points	+	24 VDC internal current consumption of simultaneously "ON" relay/transistor outputs		

If the total consumption exceeds the CPU's built-in power supply capacity range, use the extension power supply unit (A0J2PW). For the I/O units which is supplied with 5 VDC power by the extension unit, set the I/O units internal power supply select switch to "EX5V".

POINT

The allowable current capacity of the 5 VDC power supply which can be supplied from the extension power supply unit to the I/O units and extension base unit is 2.3 A. If it exceeds 2.3 A, use the extension base unit A65B.

(2) Receiving end voltage of each module

Since the 5 VDC power is supplied to the I/O units and extension base unit through the I/O cables and extension cables, respectively, the voltage may drop at the cables. Therefore, specified voltage (4.75 VDC or more) may not be supplied at the receiving end, causing input/output errors. Calculate the voltage requirement as described below and determine whether or not the A0J2PW is to be used.

1) 5 VDC power requirement

i) 5 VDC output voltage range of the power supply unit is 4.9 to 5.2 VDC.

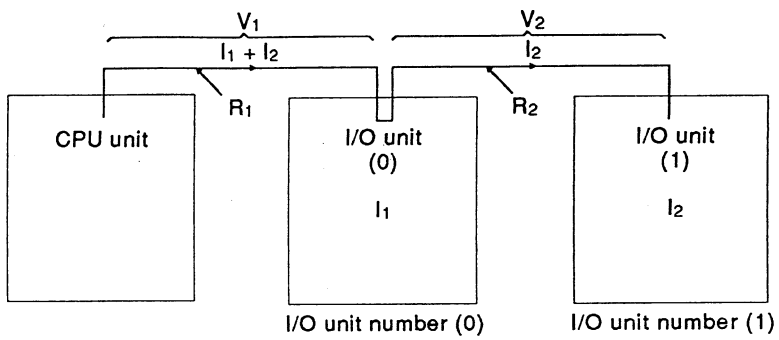
ii) The specified voltage at the I/O unit or the extension base unit is 4.75 VDC or more.

2) Cable resistances

A0J2C01	0.047 Ω
A0J2C03	0.0617 Ω
A0J2C06	0.0882 Ω

Refer to 5.2 for cable resistances.
Due to the above requirements 1) and 2), it is necessary to satisfy the specified voltage (4.75 VDC or more) of the system at the receiving end when the 5 VDC output of the power supply unit is a minimum of 4.9 VDC. Voltage calculation at the receiving end is as described on the next page.

How to calculate receiving end voltage



V_1 : Voltage drop at the cable between CPU unit and I/O unit (0)
V_2 : Voltage drop at the cable between I/O unit (0) and I/O unit (1)
R_1 : Resistance of the cable between CPU unit and I/O unit (0)
R_2 : Resistance of the cable between I/O unit (0) and I/O unit (1)
I_1 : Current consumption of the 5 VDC power in I/O unit (0)
I_2 : Current consumption of the 5 VDC power in I/O unit (1)

Fig. 10.1 System Configuration and Symbols Used

The voltage drops V_1 and V_2 are,

$V_1 = R_1 (I_1 + I_2)$

$V_2 + R_2 I_1$

The voltage at the receiving end of I/O unit (1) is,

Receiving end voltage = $4.9 - (V_1 + V_2) > 4.75$

To satisfy the requirement that the receiving end voltage must be 4.75 VDC or more,

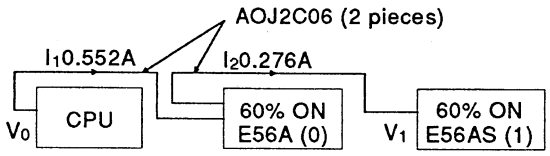
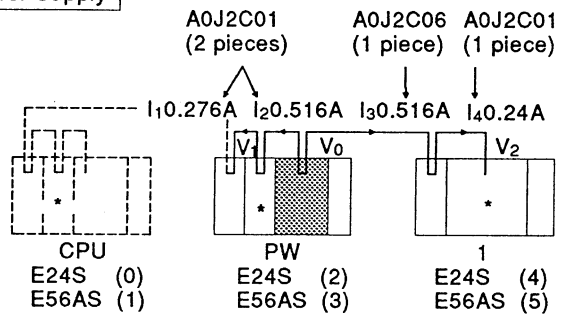
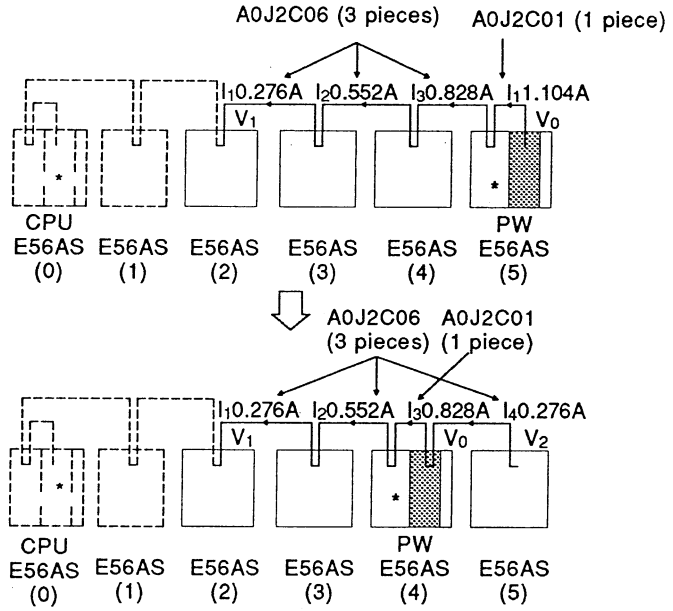
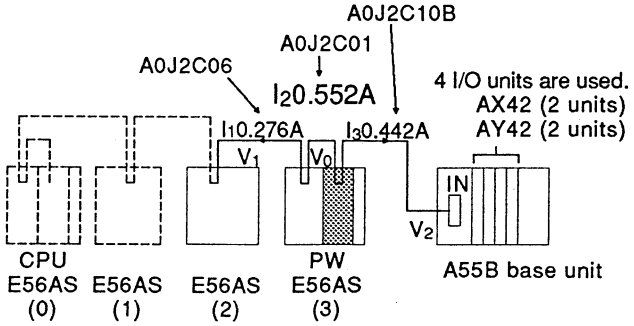
$4.9 - 4.75 > V_1 + V_2$

$0.15 > R_1 (I_1 + I_2) + R_2 I_2$

If the condition is met, extension is allowed up to the I/O unit (1).

Therefore, the number of I/O units to be extended or use of the extension base unit (A55B) can be determined when the following condition is met:
0.15(= 4.9 – 4.75) > sum of the voltage drops up to the receiving end.

(3) 5 VDC power voltage drop calculation example using A0J2 cables.

<table>
<tr><th></th><th>System Configuration</th></tr>
<tr><td>Example 1</td><td>Using CPU's Built-in Power Supply Only
112 I/O points
 
</td></tr>
<tr><td>Example 2</td><td>Using Extension Power Supply
240 I/O points
 
</td></tr>
<tr><td>Example 3</td><td>Mounting Extension Power Supply unit on I/O unit at Final End
336 I/0 points
 
</td></tr>
<tr><td>Example 4</td><td>Using Extension Base Unit
448 I/O points
 
</td></tr>
</table>

Voltage Drop	Judgment	Power Select Switch
V_1 = A0J206 Resistance x (I_1 + I_2) = 0.0882 x (0.552 + 0.276) = 0.073 (V)	0.15 V or less o	CPU 5 V position
V_1= A0J2C01 Resistance x (I_1 + I_2) = 0.047 x (0.276 + 0.516) = 0.037 (V) V_2 = A0J2C06 Resistance x I_3 + A0J2C01 Resistance x I_4 = 0.0882 x 0.516 + 0.047 x 0.24 = 0.057 (V)	o	CPU 5 V position: I/O unit 0.1 EX 5 V position: I/O units 2,3,4,5
V_1 = A0J2C01 Resistance x I_4 + A0J2C06 Resistance x (I_1+I_2+I_3) = 0.047 x 1.104 + 0.0882 x (0.276 + 0.552 + 0.828) = 0.198 (V) When the extension power supply unit is used at the final end, voltage drop at the final end unit supplied with power is large and the requirement of 0.15 V or less is not satisfied. Therefore, take the following remedy.	0.15 V or more X	CPU 5 V position: I/O units 0.1 EX 5 V position: I/O units 2,3,4,5
V_1 = A0J2C01 Resistance x I_3 + A0J2C06 Resistance x (I_1 + I_2) = 0.047 x 0.828 + 0.0882 x (0.276 + 0.552) = 0.112 (V) V_2 = A0J2C06 Resistance x I_4 = 0.0882 x 0.276 = 0.024 (V)	o	
V_1 = A0J2C06 Resistance x I_1 + A0J2C01 Resistance x I_2 = 0.0882 x 0.276 + 0.047 x 0.552 = 0.0503 (V) V_2 = A0J2C10B Resistance x I_3 = 0.126 x 0.492 = 0.062 (V)	o	CPU 5 V position: I/O units 0.1 EX 5 V position: I/O units 2,3

* Unit-to-unit mounting

1) I/O unit numbers are indicated in parentheses. I/O unit current consumption has been calculated, assuming that the simultaneous ON ratio is maximum of 60 %.

2) In Examples 2, 3, and 4, the units supplied with 5 VDC power from the extension power supply unit are indicated by the full line. The units supplied with the power by the CPU's built-in power supply are shown by the dotted line.

3) Indicated above are voltage drops occurring between the power supply unit and the I/O unit at the final end.

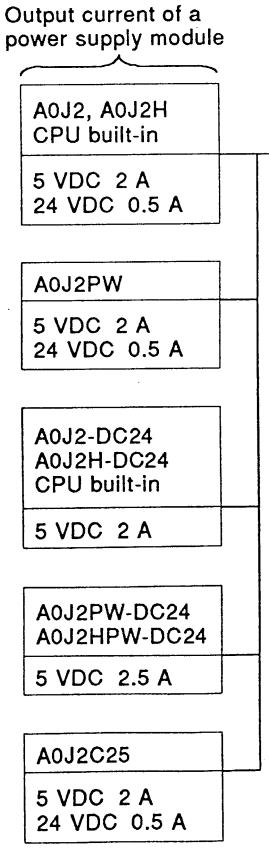
POINTS

(1) As shown in Examples 3 and 4, the voltage drop of the I/O unit are the final end varies depending on the location of the extension power supply module and the connection of the cable. Therefore, select the I/O or extension cable or select I/O unit so that the voltage drop may be 0.15 V in the system.

(2) Avoid using the extension power supply unit at the final end because the voltage drop value is larger.

(4) 24 VDC current consumption of each module

The 24 VDC output current capacity of power supply modules and the 24 VDC current consumption of all modules are shown below. If there is a shortage in the following values, use an extension power supply module or an external DC stabilized power supply.



I/O Modules and Special-Function Modules		Current Consumption (A)
A0J2-E24R	Relay contact output	0.23
A0J2-E28AR A0J2-E28DR	Relay contact output	0.125
A0J2-E56AR A0J2-E56DR	Relay contact output	0.23
A0J2-E56DR	Relay contact output	0.22
A0J2-62DA	D-A conversion	0.23
A0J2-D71	2-axis positioning	0.05

10.2 Selection of a Power Supply Module for an A1S

(1) 5 VDC current consumption of all modules

The output current capacity of power supply modules and the 5 VDC current consumption of all modules are shown below.
Select the power supply module by using the following chart.

5 VDC current consumption of an A1S module (A)

Output current of a power supply module

A1S61P
5 VDC 5 A

A1S62P
5 VDC 3 A 24 VDC 0.6 A

A1S63P
5 VDC 5 A

A1SCPU(S1)
0.4

Peripheral Devices	
A7PU	0.4
A7PUS	
A6GPP	Not consumed.
A6HGP	
A6PHP	
A7PHP	

Input Modules	
A1SX10	0.05
A1SX20	
A1SX30	
A1SX40	
A1SX40-S1	
A1SX40-S2	
A1SX41	0.08
A1SX41-S2	
A1SX42	0.09
A1SX42-S2	
A1SX80	0.05
A1SX80-S1	
A1SX80-S2	
A1SX81	0.08
A1SX81-S2	

Combined I/O /Dynamic I/O module	
A1SH42	0.50
A1S42X	0.08
A1S42Y	0.10

Output Modules	
A1SY10	0.12
A1SY18A	0.24
A1SY22	0.27
A1SY28A	0.11
A1SY40	0.27
A1SY41	0.5
A1SY42	0.93
A1SY50	0.12
A1SY60	
A1SY60E	0.20
A1SY68A	0.13
A1SY71	0.40
A1SY80	0.12
A1SY81	0.5

Special-Function Modules		
A1SD61	High-speed counter	0.35
A1S64AD	A-D conversion	0.4
A1S62DA	D-A conversion	0.8
A1S62RD3	Temperature-digital conversion	0.54
A1S62RD4		0.44
A1SJ71T21B	Data link	0.66
A1SJ71C24-R2/R4/PRF	Computer link	0.1
A1SP60	Pulse catch	0.055
A1ST60	Analog timer	
A1SI61	Interrupt	0.057

(2) Application standards of extension base unit (A1S52B, A1S55B, A1S58B, A55B, A58B)

With the A1S52B, A1S55B, A1S58B, A55B, or A58B extension base unit, 5 VDC is supplied from the power supply module of the main base unit via extension cable. Therefore, some voltage drop occurs over the extension cable and the specified voltage is not supplied to the receiving end , resulting in mis-input and mis-output.
If the voltage at the receiving end is less than 4.75 V, use an extension base unit of models A1S65B, A1S68B, A65B, or A68B equipped with a power supply unit.

(a) Selection conditions

The voltage received by the module installed in the last slot of an extension base unit A1S52B, A1S55B, A1S58B, A55B, or A58B must be 4.75 V or above.
Since the output voltage of the power supply module is set at 5.1 V or above, the voltage drop must be 0.35 V or less.

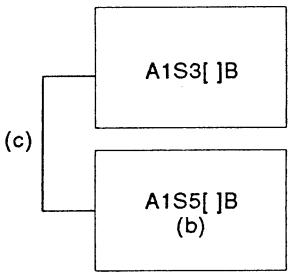
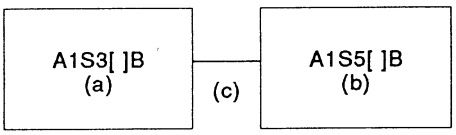
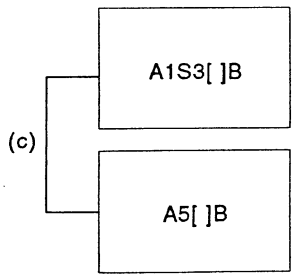
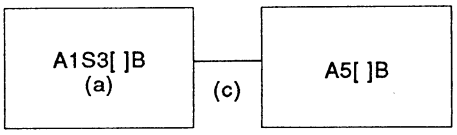
(3) Classification of voltage drop

Voltage drop is classified into (a), (b), and (c) as follows according to the connecting method and type of extension base units.

(a) Voltage drop of a main base unit

(b) Voltage drop of an extension base unit

(c) Voltage drop over an extension cable

	Extension cable connected to the left side of main base unit (serial)	Extension cable connected to the right side of main base unit (parallel)
A1S52B, A1S55B, or A1S58B extension base unit is used	 Voltage drop of the main base unit can be ignored.	
A55B or A58B extension base unit is used	 Voltage drop of the main and the extension base units can be ignored.	 Voltage drop of the extension base units can be ignored.

(4) Calculation of the receiving-end voltage

(a) Voltage drop of a main base unit (A1S32B, A1S35B, A1S38B)

Each slot of a main base unit has a resistance of 0.007 Ω.

Calculate voltage drop of each slot, and obtain the total voltage drop of a base unit.

1) Voltage drop of a CPU module: V CPU

V CPU = 0.007 x (current consumption of the CPU module: 0.4) = 0.0028 (V)

2) Voltage drop of slot 0: V K0

V K0 = 0.014 x (current consumption of the module in slot 0: I K0)

3) Voltage drop of slot 1: V K1

V K1 = 0.021 x (current consumption of the module in slot 1: I K1)

4) Voltage drop of slot 2: V K2

V K2 = 0.028 x (current consumption of the module in slot 2: I K2)

5) Voltage drop of slot 3: V K3

V K3 = 0.035 x (current consumption of the module in slot 3: I K3)

6) Voltage drop of slot 4: V K4

V K4 = 0.042 x (current consumption of the module in slot 4: I K4)

7) Voltage drop of slot 5: V K5

V K5 = 0.049 x (current consumption of the module in slot 5: I K5)

8) Voltage drop of slot 6: V K6

V K6 = 0.056 x (current consumption of the module in slot 6: I K6)

9) Voltage drop of slot 6: V K7

V K7 = 0.063 x (current consumption of the module in slot 7: I K7)

10) Voltage drop of a base unit: V K

V K = V CPU + V K0 + V K1 + V K2 + V K3 + V K4 + V K5 + V K6 + V K7

(b) Voltage drop of an extension base unit (A1S52B, A1S55B, A1S58B)

Each slot of an extension base unit has a resistance of 0.006 Ω. Calculate voltage drop of each slot, and obtain the total voltage drop of a base unit.

1) Voltage drop of slot 0: V Z0

V Z0 = 0.006 x (current consumption of the module in slot 0: I Z0)

2) Voltage drop of slot 1: V Z1

V Z1 = 0.012 x (current consumption of the module in slot 1:

3) Voltage drop of slot 2: V Z2

V Z2 = 0.018 x (current consumption of the module in slot 2: I Z2)

4) Voltage drop of slot 3: V Z3

V Z3 = 0.024 x (current consumption of the module in slot 3: I Z3)

5) Voltage drop of slot 4: V Z4

V Z4 = 0.030 x (current consumption of the module in slot 4: I Z4)

6) Voltage drop of slot 5: V Z5

V Z5 = 0.036 x (current consumption of the module in slot 5: I Z5)

7) Voltage drop of slot 6: V Z6

V Z6 = 0.042 x (current consumption of the module in slot 6: I Z6)

8) Voltage drop of slot 6: V Z7

V Z7 = 0.048 x (current consumption of the module in slot 7: I Z7)

9) Voltage drop of an extension base unit: V Z

V Z = V Z0 + V Z1 + V Z2 + V Z3 + V Z4 + V Z5 + V Z6 + V Z7

(c) Voltage drop over extension cables

1) Total current consumption of an extension base unit: I Z

I Z = I Z0 + I Z1 + I Z2 + I Z3 + I Z4 + I Z5 + I Z6 + I Z7

2) Voltage drop over an extension cable: V C

V C = (Resistance of an extension cable) x I Z

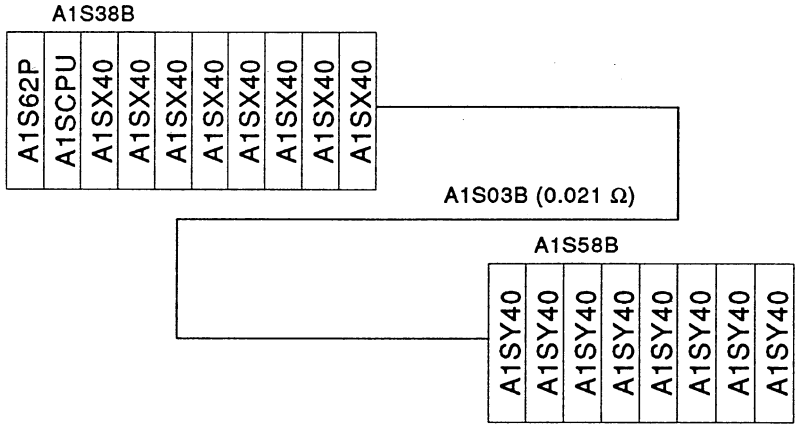
Resistance of an extension cable

A1SC01B : 0.02 Ω
A1SC03B : 0.021 Ω
A1SC12B : 0.055 Ω
A1SC30B : 0.121 Ω
A1SC05NB: 0.037 Ω

(d) Voltage at the receiving end

(5.1 (V) – VK – VZ – VC) ≥ 4.75 (V)

Example



1) Voltage drop of a main base unit

VK = 0.007 x 0.4 + (0.014 x 0.05 + 0.021 x 0.05 + 0.028 x 0.05 + 0.035 X 0.05 + 0.042 x 0.05 + 0.049 x 0.05 + 0.056 x 0.05 + 0.063 x 0.05) = 0.0182 (V)

2) Voltage drop of an extension base unit

VZ = 0.006 x 0.27 + (0.012 x 0.27 + 0.018 x 0.27 + 0.024 x 0.27 + 0.030 x 0.27 + 0.036 x 0.27 + 0.042 x 0.27 + 0.048 x 0.27) = 0.05832 (V)

3) Voltage drop over an extension cable

VC = 0.021 x (0.27 x 8) = 0.04536 (V)

4) Voltage at the receiving end

5.1 – 0.0182 – 0.05832 – 0.04536 ≠ 4.978 (V)
Since the voltage at the receiving end is more than 4.75 V, the above system can be put into operation.

(5) 24 VDC current consumption of all modules

The 24 VDC output current consumption of power supply modules and the 24 VDC current consumption of all modules are shown below. If there is a shortage in the following values, use an external DC stabilized power supply.

Output current of a power supply module

A1S61P	5 VDC 5 A
A1S62P	5 VDC 3 A 24 VDC 0.6 A

Output Modules		Current Consumption (A)
A1SY10	Relay contact output	0.09

10.3 Selection of an Extension Power Supply Module for an A2CCPU

(1) 5 VDC current consumption of all modules

5 VDC is supplied by the 24 VDC power supply of each module. Therefore, it is unrelated to the selection of power supply modules.

(2) 24 VDC current consumption of all modules

The 24 VDC output current capacity of power supply modules and the 24 VDC current consumption of all modules are shown below. If there is a shortage in the following values, use an extension power supply module or an external DC stabilized power supply.

[Some MELSECNET/MINI-S3 remote I/O modules can be used as I/O modules for an A2C. See Table 2.1 of the A2CCPU User's Manual.]

A2CCPU
A2CCPUC24(PRF)
———

A66P
24 VDC 0.6 A

A2C I/O Modules (A)	
AX11C	0.056
AX21C	0.058
AX31C	0.056
AX41C	0.055
AX81C	0.055
AY13C	0.09
AY23C	0.18
AY51C	0.093
AY61CE	0.15
AY81C	0.1
AX10Y10C	0.092
AX40Y10C	0.092
AX10Y22C	0.116
AX40Y50C	0.074
AX80Y10C	0.092
AX80Y80C	0.082

A2C Special-Function Modules (A)	
A68ADC	0.3
AD61C	0.15
AD62C	0.15
A64DAIC A64DAVC	0.12
A64RD3C	0.2
A64RD4C	0.15

10.4 Selection of a Power Supply Module for an A1, A2, and A3 Type CPU

(1) 5 VDC current consumption of each module

The current consumption capacity of power supply modules and the 5 VDC current consumption of all modules are shown below. Select power supply modules by using the following chart.

5 VDC current consumption of each module (A)

Output current of a power supply module

A61P 5 VDC 8 A
A62P 5 VDC 5 A 24 VDC 0.8 A
A63P (24 VDC input) 5 VDC 8 A
A65P 5 VDC 2 A 24 VDC 1.5 A
A66P 24 VDC 1.2 A
A1CPU A1NCPU 5 VDC 5 A 24 VDC 0.8 A

CPU Types	For Single	For Optical Link (P21)	For Coaxial Link (R21)
A1CPU	1.5	3.4	3.7
A2CPU	1.6	3.5	3.8
A2CPU-S1	1.6	3.5	3.8
A3CPU	1.7	3.6	3.9
A3HCPU	3.1	3.7	4.1
A1NCPU	0.53	1.23	1.63
A2NCPU	0.73	1.38	1.78
A2NCPU-S1	0.73	1.38	1.78
A3NCPU	0.90	1.55	1.95
A2ACPU	0.4	1.0	1.4
A2ACPU-S1	0.4	1.0	1.4
A3ACPU	0.6	1.1	1.6

Input Modules	
AX10 AX20 AX40 AX50 AX50-S1 AX60 AX60-S1 AX70 AX80 AX80E	0.06
AX11 AX21 AX41 AX71 AX81	0.11
AX42 AX82	0.11

Dynamic Combined I/O Module	
A42XY	0.11

Output Modules	
AY10 AY10A AY11 AY11A AY11E	0.12
AY13 AY13E	0.23
AY22	0.31
AY23	0.59
AY40	0.12
AY40A	0.19
AY41	0.23
AY42	0.29
AY50 AY60 AY60E AY80	0.12
AY60S1	0.08
AY60EP AY80EP	0.12
AY51 AY81	0.23
AY70	0.1
AY71	0.2
AY81EP	0.23
AY82EP	0.29

Special-Function Modules		
AI61	Interrupt	0.14
A11VC	Audio output	0.6
AD61 (S1)	High-speed counter	0.3
A68AD/A68ADS2	A-D conversion	0.9
A84AD	A-D and D-A conversion	0.24
A62DA/A62DAS1	D-A conversion	0.6
AD70	Positioning	0.3
AD71 (S1) (S7)		1.5
AD71S2		1.5
A61LS/A62LS	Position detection	0.8/1.5
AD72	Positioning	0.9
AD76		————
A616AD/A60MX(R)	A-D conversion	1/0.5
A616TD/A60MXT	Temperature-digital conversion	1/0.8
A616DAI/A616DAV	D-A conversion	0.3/0.38
AJ71P22/R22	Data link	1.9/2.2
AJ72P25/R25		2.3/2.6
AJ71P32/T32	Data link (MINI)	0.23/0.26
AJ71C22	Multidrop link	1.4
AJ71C24 (S3) (S6) (S8)	Computer link	1.4
AD51 AD51S3/AD51H	Communications	1.3/1.0
AD57/AD57S1/AD57G (S3)	Control	1.21/1.55/1.1
AD58		1.3
AJ71PT32-S3	MELSECNET/MINI-S3	0.35
AJ71B62	B/NET interface	0.17
AJ71P41	SUMINET interface	0.4/0.7 (Without power supply equipment)
AD71C21/AJ71C21S1	Terminal interface	0.8
AD59/AD59-S1	Memory card centronics interface	0.3

Peripheral Devices	
A7PU/A7PUS	0.4
A8PUE	0.4
A6WU	0.8
AD71TU	0.3
A6GPP	Not consumed.
A6HGP	
A6PHP	
A7PHP	

(2) Application standard for an extension base which does not need a power supply module

With the Type A55B or A58B extension base unit, 5 VDC is supplied from the power supply module of the main base unit via the extension cable. Therefore, some voltage drop occurs over the extension cable and the specified voltage is not supplied to the receiving end, resulting in mis-input and mis-output. It is recommended that the A55B and A58B units be connected behind the main base unit to minimize voltage drop. Select the availability by calculations using the following selection conditions:

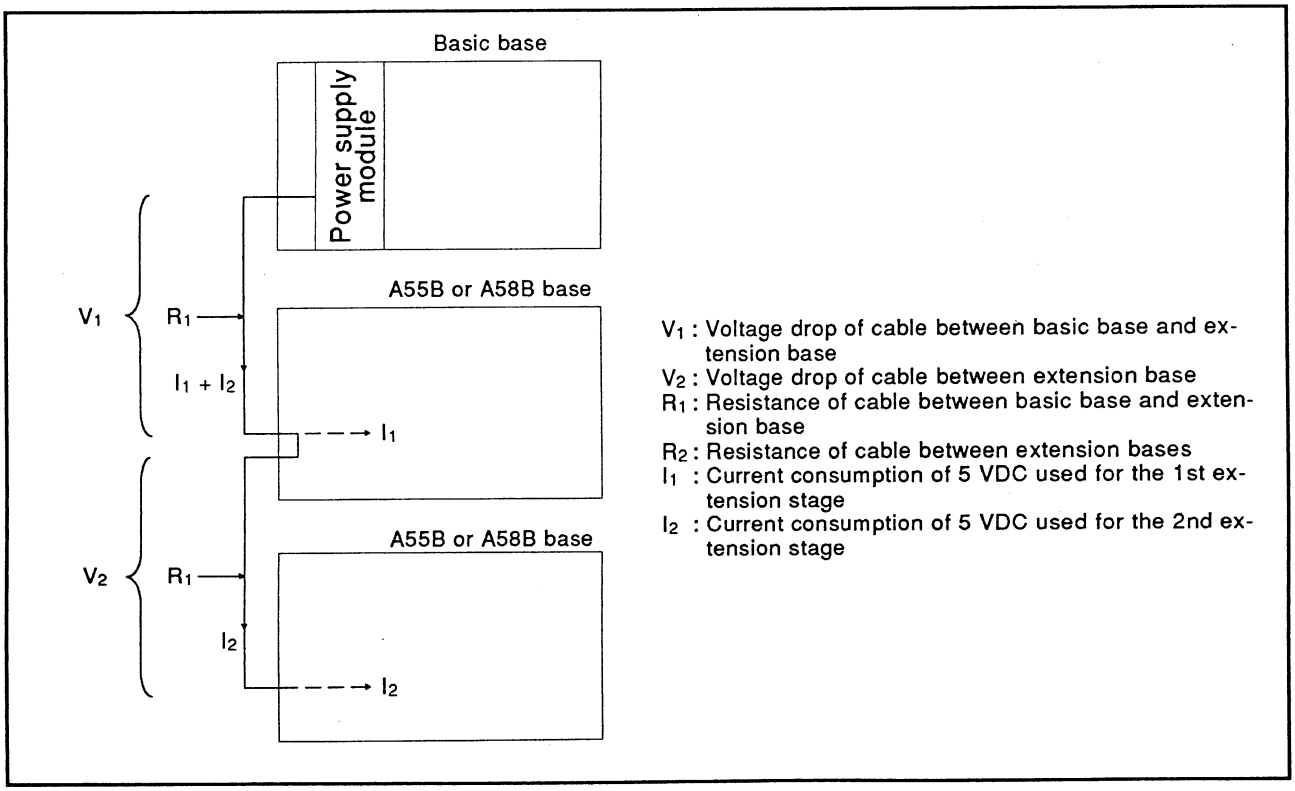
(a) Selection conditions

1) The 5 VDC output voltage of a power supply module is 4.9 V or greater.
2) 4.75 VDC or greater at the receiving end of a base unit
3) The overall distance of an extension cable is 6.6 m or less.

(b) How to calculate receiving end voltage

Resistance value of cable

AC06B: 0.019 Ω
AC12B: 0.028 Ω
AC30B: 0.052 Ω



Voltage drops V_1 and V_2 are:

$$V_1 = R_1 (I_1 + I_2)$$
$$V_2 = R_2 I_2$$

The voltage of receiving end at the 2nd extension stage must satisfy the following expression:

Farthest base voltage = $4.9 - (V_1 + V_2) > 4.75$

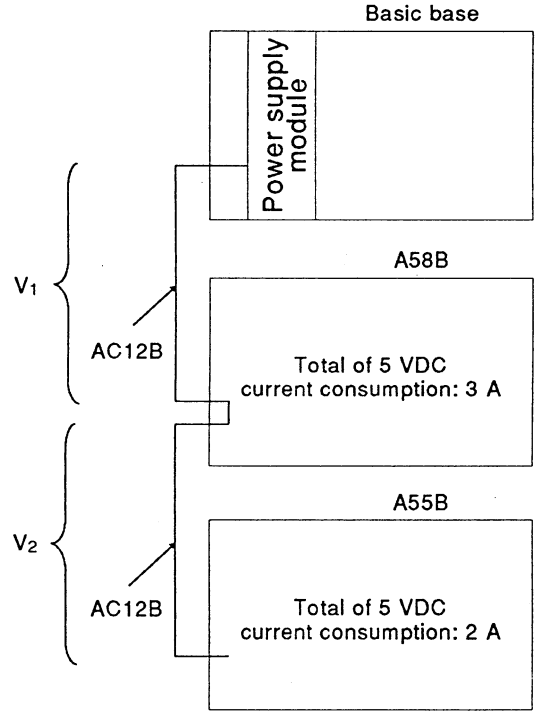
In order to satisfy the condition that the voltage at the final stage should be 4.75 V or more, the following conditions should hold:

$4.9 - 4.75 \geq V_1 + V_2$
$0.15 \geq R_1 (I_1 + I_2) + R_2 I_2$

Under the above conditions, the A55B or A58B can be used for two extension stages. Therefore, the number of A55B or A58B extension modules which may be powered from one power supply is limited by the voltage drop between the main base unit and the farthest base unit.

$0.15 \geq$ total of voltage drop up to receiving end

Calculation example



Resistance value of AC12B = 0.028 Ω

$V_1 = 0.028 \times (3 + 2) = 0.14$ [V]
$V_2 = 0.028 \times 2 = 0.056$ [V]

$V_1 + V_2 =$ 0.196 [V]

Receiving end voltage of 2nd extension stage is
4.9 - 0.196 = 4.704 V

Therefore, since the voltage drop is the 0.15 or more, the A55B cannot be used at the 2nd extension stage on this condition. In this case, the A55B can be used by changing the cable to AC06B. (Resistance value = 0.019 Ω)

$V_1 = 0.019 \times (3 + 2) = 0.095$ [V]
$V_2 = 0.019 \times 2 = 0.038$ [V]

$V_1 + V_2 = \underline{0.133\ [V]}$

[Receiving end voltage of 2nd extension stage is
4.9 - 0.133 = 4.707 V]

Thus, since the voltage drop is 0.15 V or less, the A55B can be used for the 2nd extension stage on this condition.

POINT

When using I/O modules and special function modules of which internal current consumption is large, load such modules into an extension base (A65B, A68B) which requires a power supply module.

(3) 24 VDC current consumption of each module

The 24 VDC output current capacity of power supply modules and the 24 VDC current consumption of all modules are shown below. If there is a shortage in the following values, use an external DC stabilized power supply.

Output current of a power supply module

A61P	5 VDC 8 A
A62P	5 VDC 5A 24 VDC 0.8 A
A63P (24 VDC input)	5 VDC 8 A
A65P	5 VDC 2 A 24 VDC 1.5 A
A66P	24 VDC 1.2 A
A1CPU	5 VDC 5 A 24 VDC 0.8 A

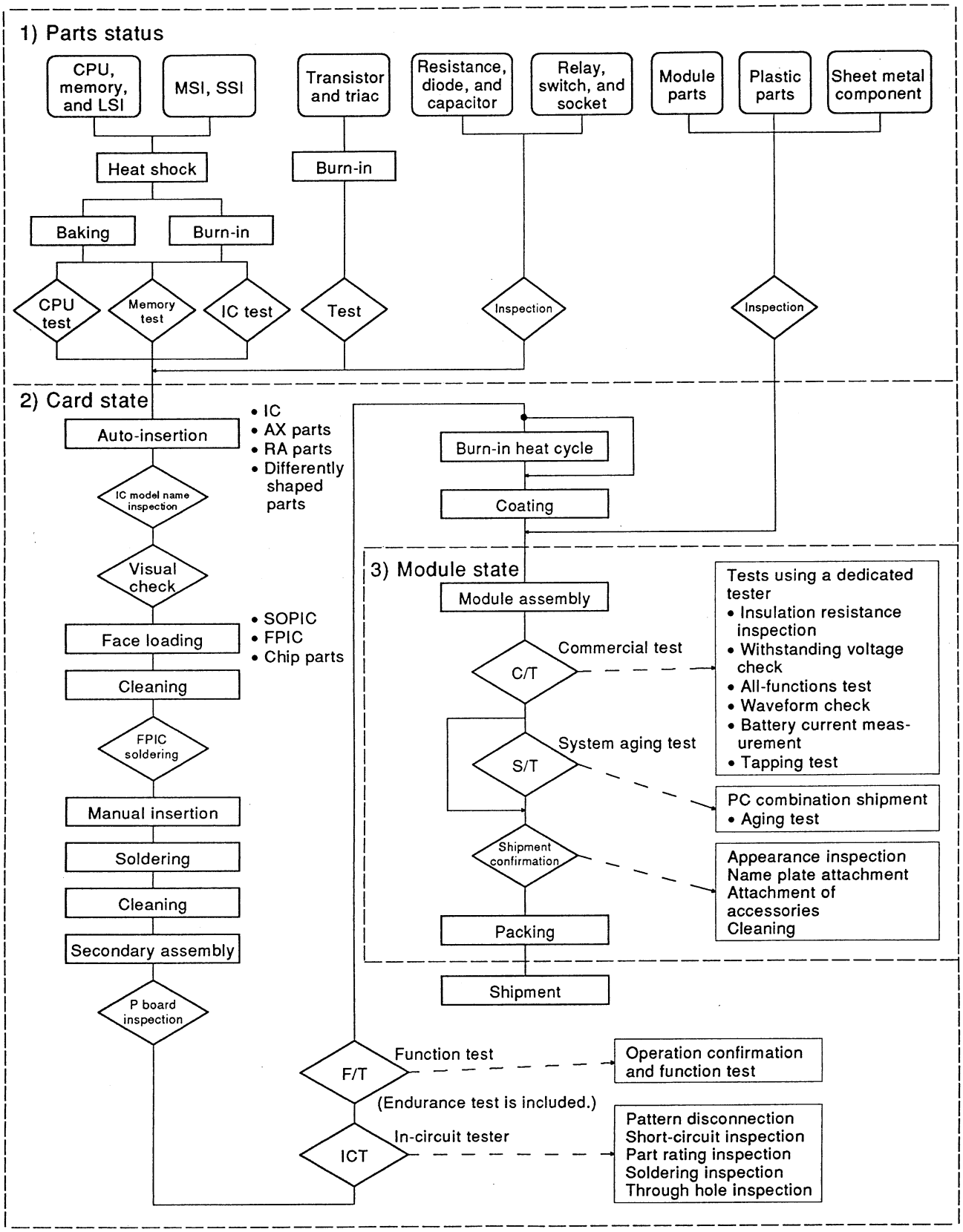
Input Modules		Current Consumption (A)
AY10 AY10A AY11 AY11A AY11E	Relay contact output	0.15
AY13 AY13E	Relay contact output	0.29

Special-Function Modules		Current Consumption (A)
A62DA	D-A conversion	0.35
AD70	1-axis positioning	0.20
A11VC	Audio output	0.33
A84AD	A-D/D-A conversion	0.53

APPENDIX

APPENDIX 1 MELSEC-A QC Process Chart

Mitsubishi PC MELSEC-A series QC process chart



	QC Processes	Inspection and Test Items	Inspection Contents, Conditions, etc.
Individual part level	Part acceptance inspection	Heat shock	Varies according to the rating of individual parts. Execute at the upper and lower limits of the storage temperature. (ex. -40 °C/+150 °C, etc.)
		Burn-in	When power is supplied, perform tests at the max. allowable temperature of the individual parts.
	Total inspection of IC and special management parts	Baking	When power is not supplied, perform tests at the max. storage temperature of the individual parts.
		Function test	Confirm all functions by using individual parts programs.
Card level	P board visual inspection	Part model name inspection	Check the part model name on the printed card.
	Except the check by ICT of post process (total inspection)	Part installation state inspection	Secure the polarity of the parts and the installation state.
		Soldering state inspection	Check all the places to be soldered.
	ICT In-circuit board tester	Check for disconnections and ladder short circuits Part polarity and rating checks	Check for P board pattern disconnection, short circuits and check part polarities and ratings.
	Heat cycle (general)	Power heat cycle test	Perform a test for 24 hours or more at the upper and lower limits of allowable ambient temperatures.
	Function test (All types of the A and LM series, and part of the K series)	Operation confirmation function test	Function test by using a dedicated tester
Module level	DIP test Noise test (Products when they are delivered at the first time)	Power supply voltage fluctuation	Test functions at 85 % of the rated voltages
		Noise application test	Apply a specified noise to an AC power input terminal, and perform the test.
		Momentary power failure test	Confirm the function by performing a momentary power failure for the specified time.
	Commercial test (total)	Function test	Test all functions and characteristics by using a dedicated tester.
		Insulation resistance inspection (specific model)	Check whether it is 5 MΩ or more by using a 500 VDC insulator.
		Withstanding voltage test (100 VAC ladder)	Apply 180 VAC for 1 sec, and perform the test. (Set current: 10 mA)

MEMO

TROUBLESHOOTING

CONTENTS

1. GENERAL INFORMATION ABOUT A-SERIES SYSTEMS

This section explains the contents, the causes, and corrective actions to take for the various errors which can occur when an ACPU system is used.

1.1 Basic Troubleshooting

System reliability not only depends on reliable equipment but also on short down-times in the event of faults.

The three basic points to be kept in mind in troubleshooting are:

(1) Visual checks

Check the following points

(a) Machine motion (in stop and operating states)

(b) Power ON or OFF

(c) Status of I/O equipment

(d) Condition of wiring (I/O wires, cables)

(e) Display states of various indicators (such as POWER LED, RUN LED, ERROR LED, and I/O LED)

(f) States of various setting switches (such as extension base and power failure compensation)

After checking (a) to (f), connect the peripheral device and check the running status of the PC CPU and the program contents.

(2) Trouble check

Observe any changes in the error condition during the following:

(a) Set the RUN keyswitch to the STOP position.

(b) Reset using the RESET keyswitch.

(c) Turn the power ON and OFF.

(3) Narrow down the possible causes of the trouble

Deduce where the fault lies, i.e:

(a) Inside or outside the PC CPU.

(b) I/O module or another module.

(c) Sequence program.

REMARK

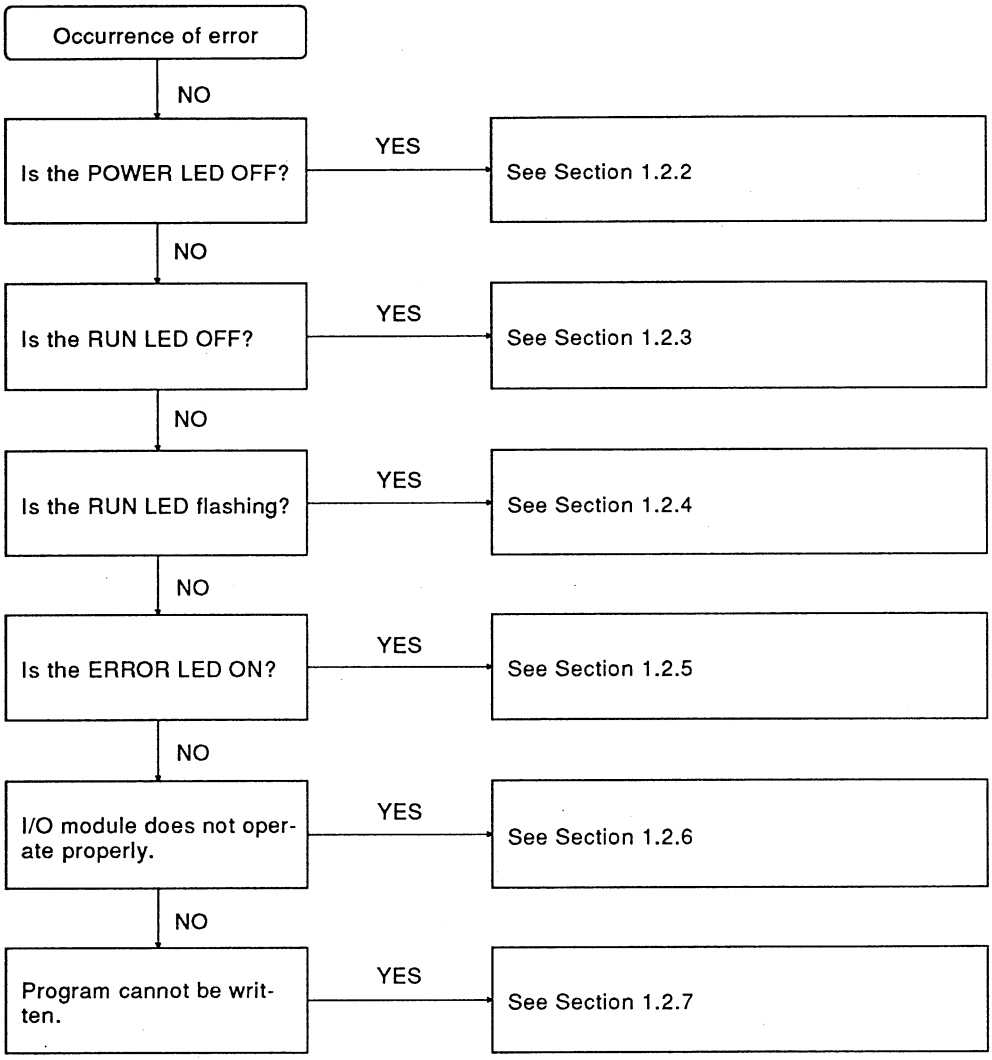
The following abreviations are used in this manual:
GPP : A6GPP type intelligent GPP
HGP : A6HGP type handy graphic panel
PHP : A6PHP plasma handy graphic panel
PU : A6PU type and A7PU type programming module
ACPU : A-series PC CPU

1.2 Troubleshooting

This section explains the procedure for determining the cause of problems as well as the errors and corrective actions for error codes.

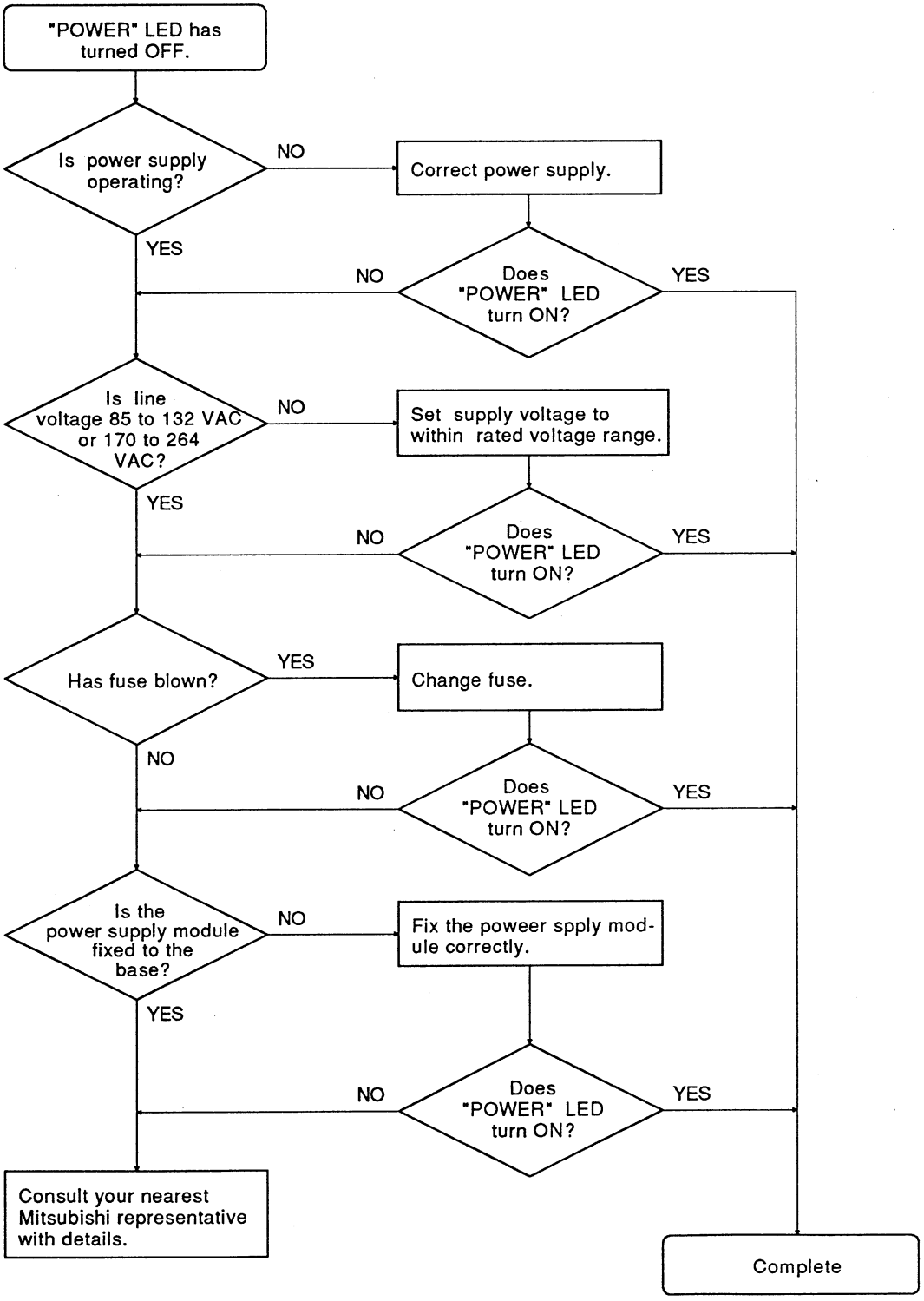
1.2.1 Troubleshooting flow chart

The procedures for troubleshooting are given in the following flow chart:



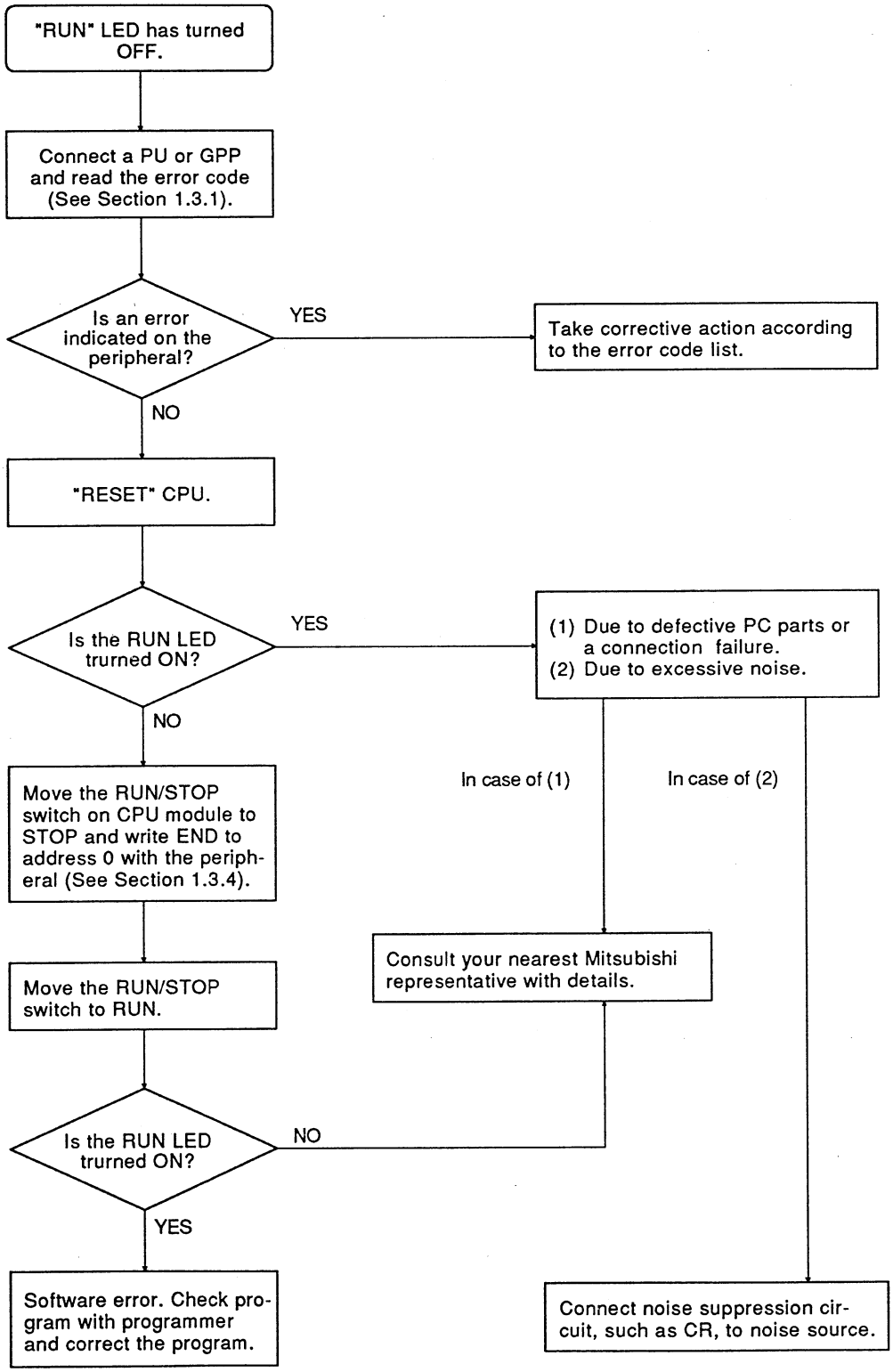
1.2.2 Flow chart used when the "POWER" LED has turned off

This section explains the flow chart when the "POWER" LED has turned off at power on or during operation.
In such cases, the cause could be one of the following:
1) Power supply voltage has dropped.
2) Power supply fuse is blown.
3) Hard ware fault in the power supply module.



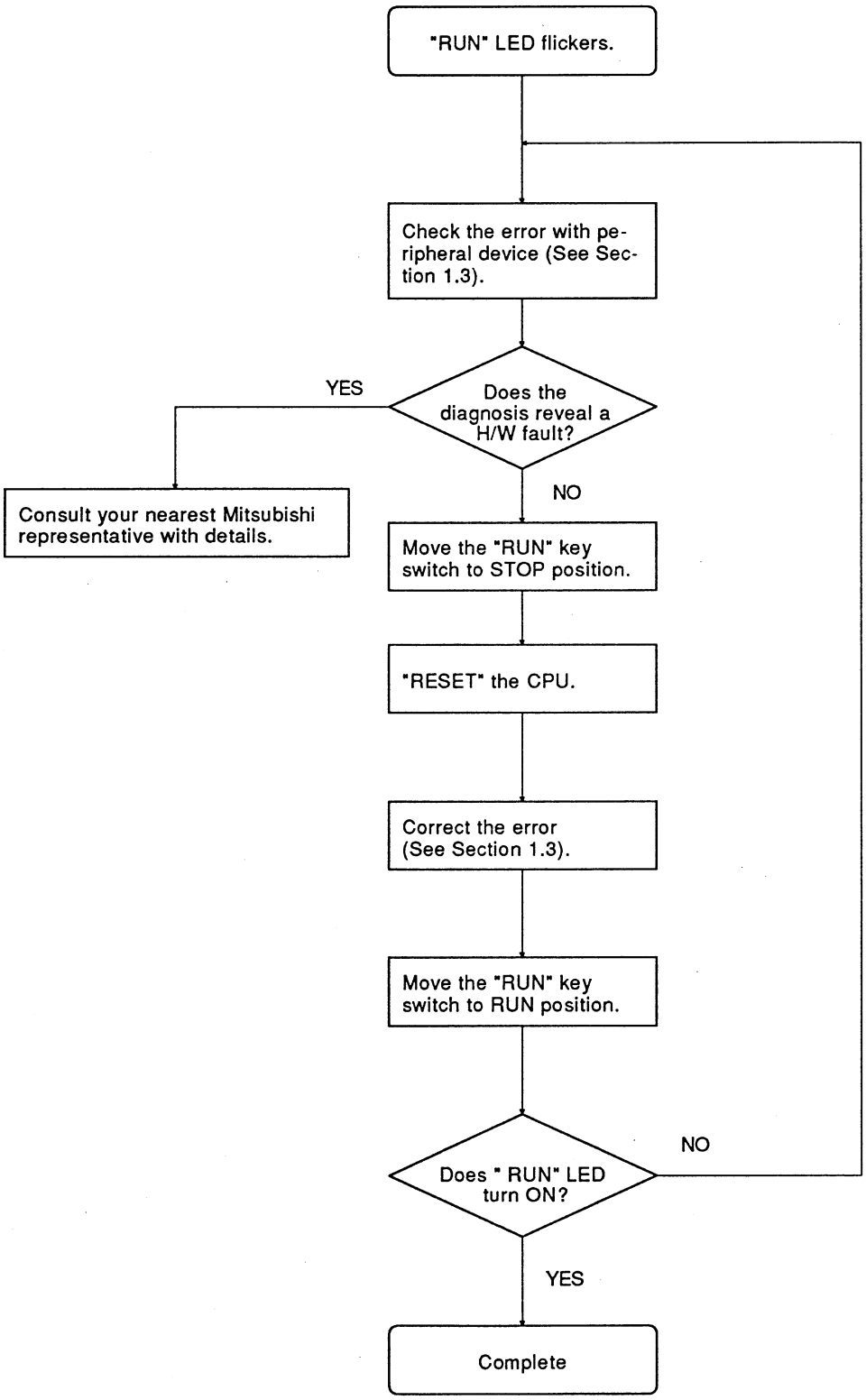
1.2.3 Flow chart used when the "RUN" LED has turned off

This section explains the flow chart when the "RUN" LED has turned off during operation.



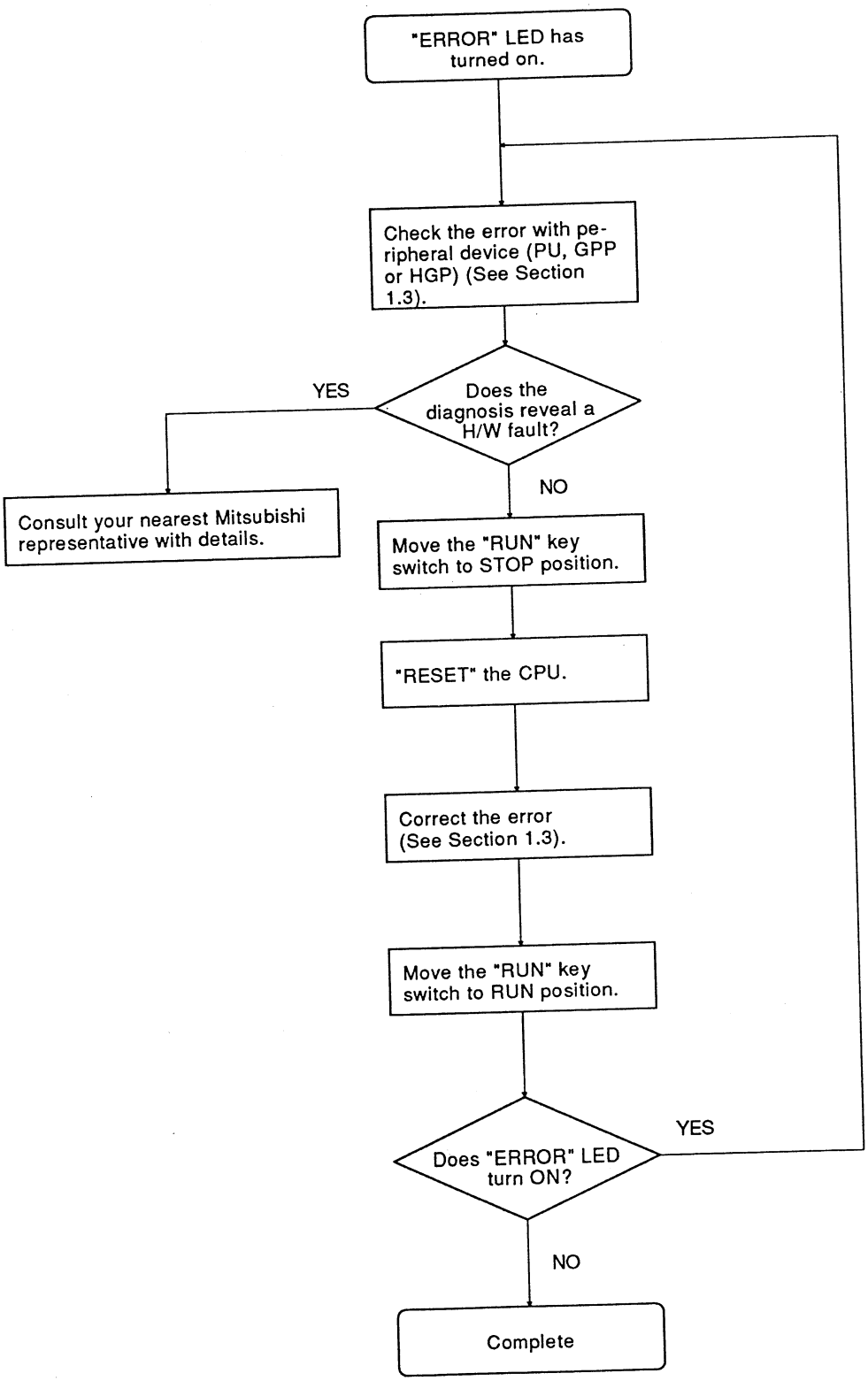
1.2.4 Flow chart used when the "RUN" LED flickers

The following flowchart shows the procedure when the RUN LED goes ON when the power supply is turned ON or when operations are started. However, in the case of an A3CPU, an error message is displayed, check and make corrections according to the error code list of Section 1.3.



1.2.5 Flow chart used when "ERROR" LED has turned on (only A1 and A2 CPUs)

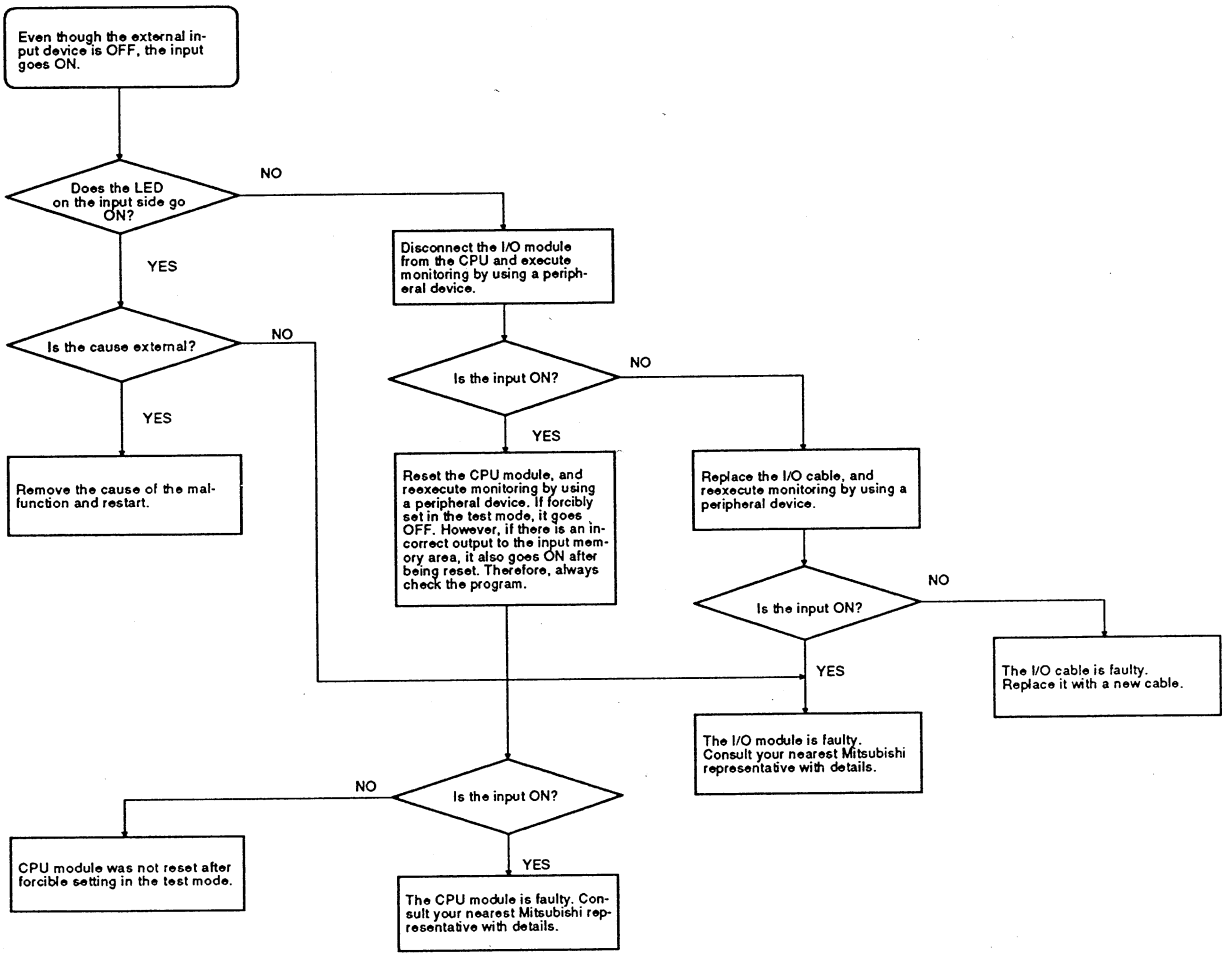
This section explains the flow chart when the "ERROR" LED come on at power-on or at the start off or during operation. (In the case of A3CPU, an error message is displayed on the LED indicator located on the front face of the CPU. Therefore, correct the error in accordance with the error massage, referring to the "error code list" in Section 1.3.)



1.2.6 I/O module troubleshooting

This section explains I/O module troubleshooting.

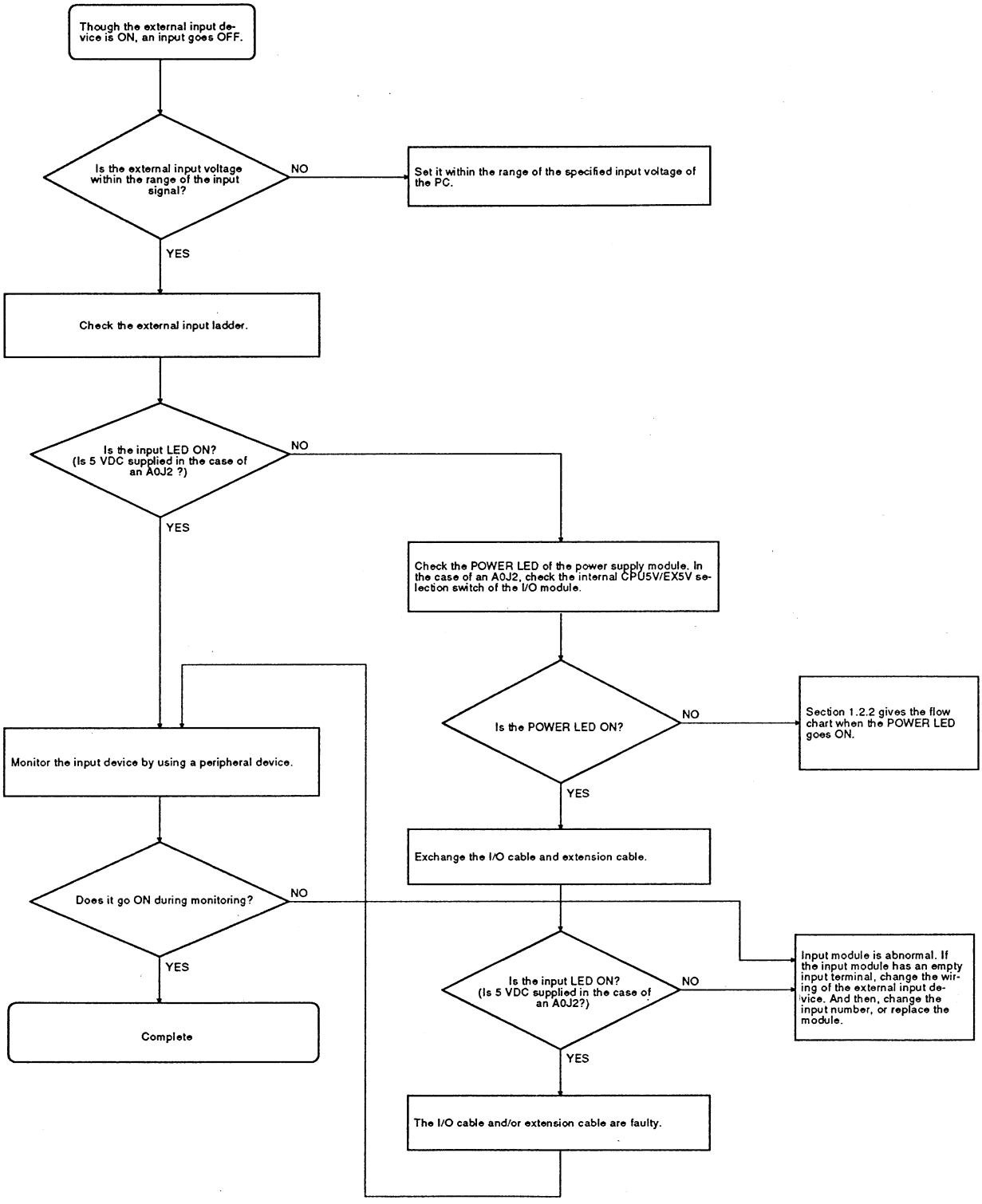
(1) Flow chart when the PC side input goes ON even though the external input device is OFF



POINT

An external factor can be a faulty external device, faulty external power supply, bad wiring, or noise.

(2) The following flow chart explains what happens if the PC side input goes ON when the external input device is ON.



(3) The following flow chart explains what happens when the load of an output module does not go ON during operations.

In such cases, the cause could be one of the following:

1) Wiring malfunction on the load side, or faulty power supply or load

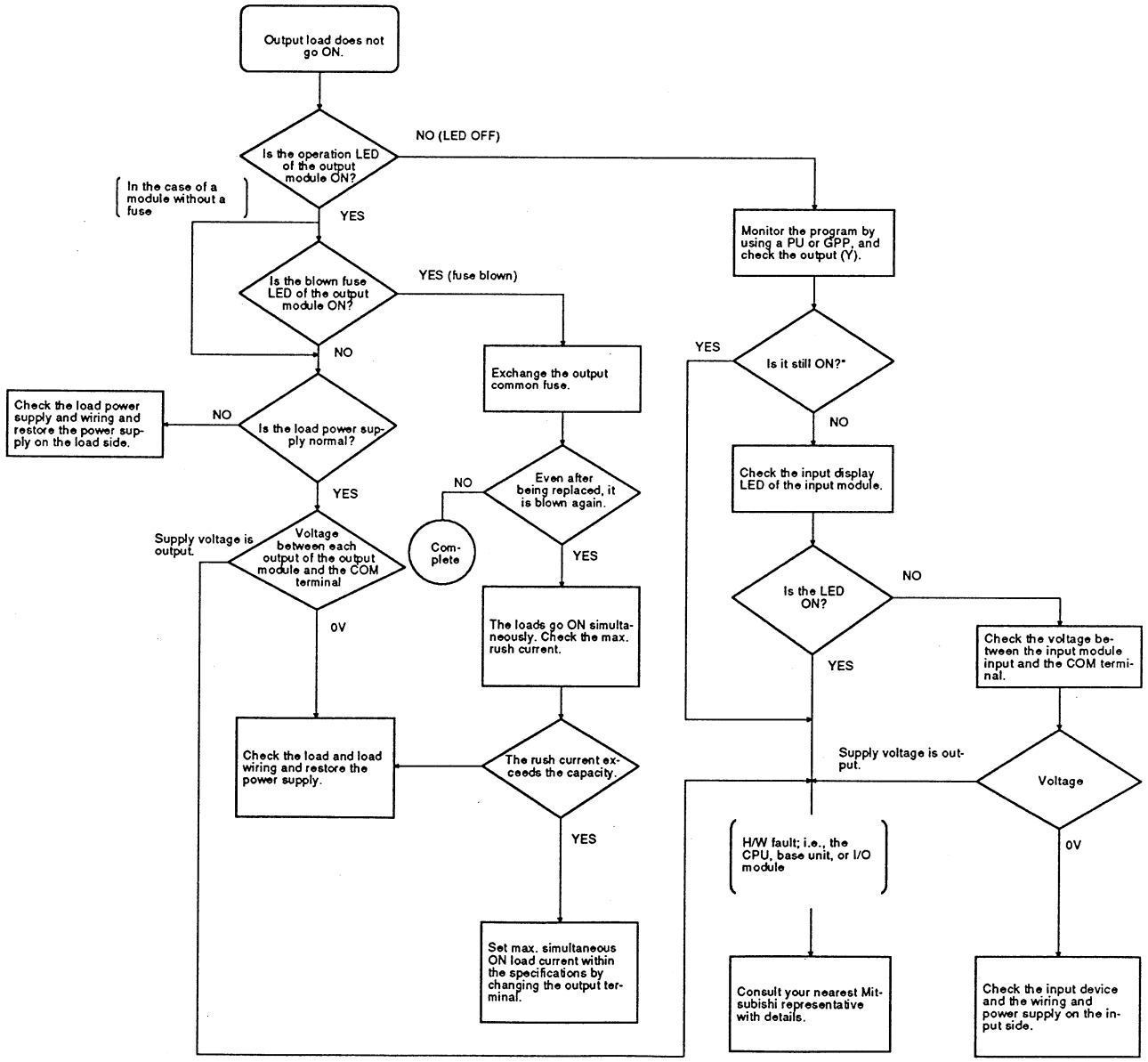
2) Faulty output module or blown fuse in the output module

3) H/W fault; i.e., the CPU, base unit, or cable

4) Program malfunction

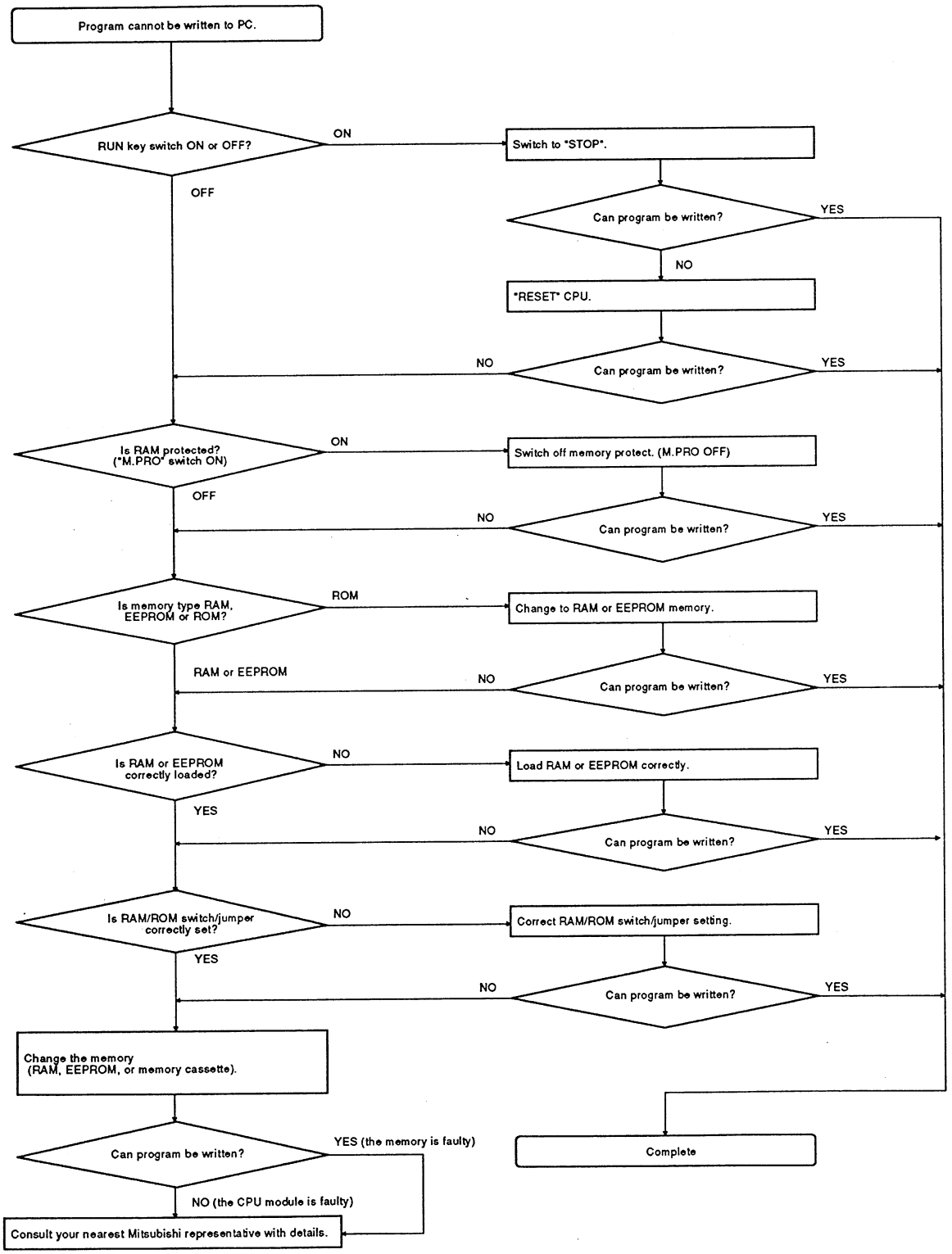
5) Faulty input module

6) Malfunction in the input device or in the wiring/power supply on the input side



1.2.7 Flow chart used when a program cannot be written to the programmable controller

This section explains flow chart when program cannot be written to the CPU (The memory EEPROM in the following flow chart is used only with an A0J2 or A1 type CPU).



1.3 Error Codes

When an error occurs in the PC RUN or RUN state, the error which is displayed or error code (including the step number) is stored in a special register (D9008) by the self-diagnostic function. This section explains how to read the error codes when an error occurs, their causes, and corrective actions to take. Perform the proper corrective action and remove the error cause.

1.3.1 How to read error codes

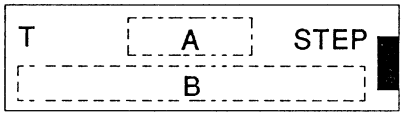
When an error occurs, error codes can be read by using an A7PU, A6GPP, A6HGP, or A6PHP.

(1) When an A7PU is used

Operations [TEST] [DEC K] [STP +] or [TEST] [DEC K] [STP -]

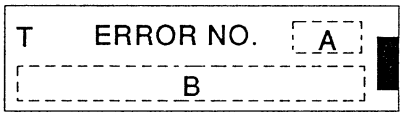
The following is displayed on a LCD screen by these key operations:

■ When the error code is 10, 13, 46, or 50.



A: Error step number (5-digit max.)
B: Error message

■ In the case of an error code other than those above

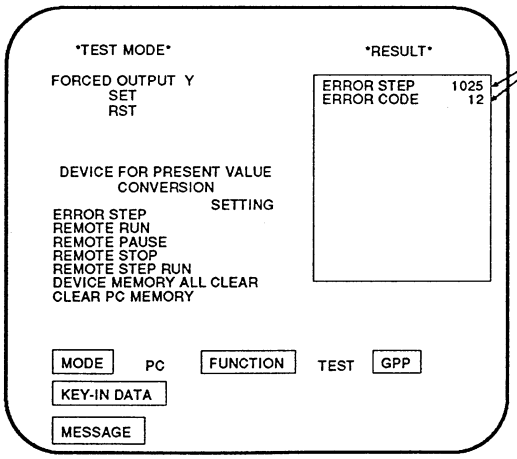


A: Error code
B: Error message

(2) When an A6GPP, A6HGP, or A6PHP is used

Operations [PC] [TEST] (Select the error step.) [GO] ----- [GO]

Error codes are displayed sequentially by using the [GO] key.



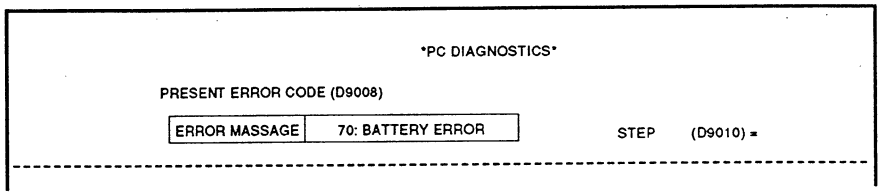
Error code or error step

When the error code is 10, 13, 46, or 50, the error step number is displayed.
In the case of other error codes, use the following method to perform PC diagnosis to check the error message that corresponds to an error code:

Operations [LST] [MNT] [↓] [GO]

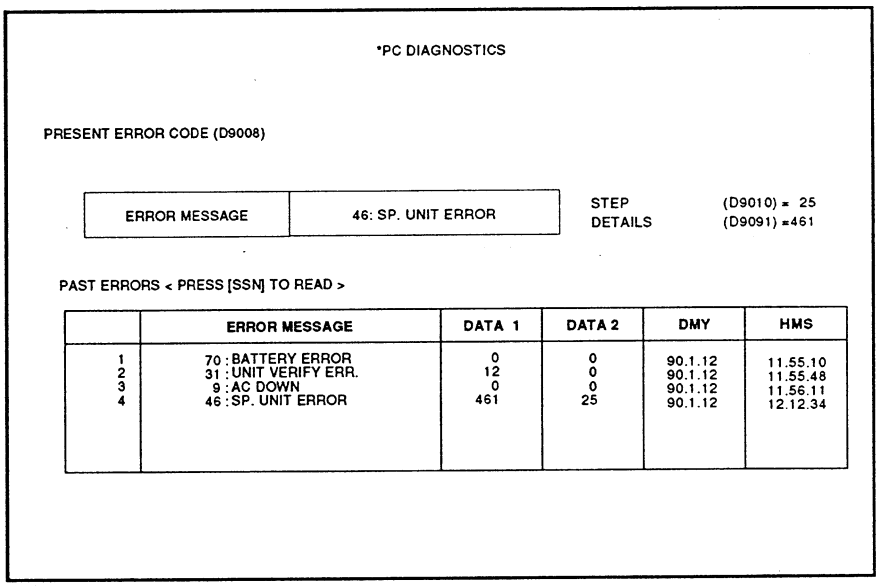
└---→ The cursor key is moved to PC DIAGNOST

In the case of other than an A2A and an A3ACPU



In the case of an A2A and A3ACPU

A list of 16 items max. of past history can be displayed by pressing the [Setting] key.



Error codes can be also checked by using a peripheral device to monitor the contents of special registers D9008, D9010, and D9091.

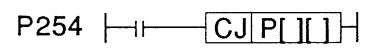
1.3.2 Error code list

When an error occurs at PC RUN or during RUN or during RUN, the error is displayed or error code is stored in special register D9008, the detailed error code is stored in special register D9011 by the self-diahnostic function. The error content and corrective action are shown in Table below.

Only the A2ACPU and A3ACPU have detailed error code (D9091).
The A0J2 type CPU does not have a * symbol.

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"INSTRCT CODE ERR." (Checked at STOP → RUN during instruction execution)	10	101	An unrecognized instruction code is being used.	(1) Read the error step by peripheral device and correct the program of that step. (2) Check to see if ROM has an undecodable instruction code and replace with ROM which has the correct content.
		102	Index is qualifying for a 32-bit constant.	Read the error step by peripheral device and correct the program of that step.
		103	The device specified by extension application instruction is incorrect.	
		104	The program structure of the extension application instruction is incorrect.	
		105	The command name of the extension application instruction is incorrect.	
		106	There is a place where index qualifying with Z or V is made in the program in [LEDA/B|IX] to [LEDA/B|IXEND].	
		107	(1) The device number and set value in the OUT instruction of the timer and counter are qualified by an index. (2) The label number of pointer (p) assigned to a destination head of [CJ], [SCJ], [CALL], [CALLP], [JMP], [LEDA/B|FCALL], [LADA/B|BREAK] instructions or the label number of interrupt pointer (I) assigned to an interrupt program head is qualified by an index.	
		108	Error other than 101 to 107 above	

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"PARAMERER ERROR" (Checked at power-on, STOP → RUN, and PAUSE → RUN)	*11	111	The capacity settings of the main program, subprograms, microcomputer programs, file register comments, status latch, dampling trace or extension file registers are not within the usable CPU range.	Read the paramerers in the CPU memory and rewrite to the memory after checking and correcting the content.
		112	The total of the set capacities of the main program, subprograms, file register comments, status latch, sampling trace and extension file registers exceed the memory cassette capacity.	
		113	The latch range in paramerers or the M, L, S setting is incorrect.	
		114	Sum check error	
		115	Paramter remote RUN/PAUSE contacts, the run mode at error occurrence, the annunciator display mode or the STOP → RUN display mode settings are incorrect.	
		116	Parameter MNET-MINI automatic refresh setting is incorrect.	
		117	Parameter timer settings are incorrect.	
		118	Parameter counter settings are incorrect.	
"MISSING END INS." (Checked at STOP → RUN)	12	121	There is no END (FEND) instruction in the main program.	Write END in main program.
		122	Subprogram has been allocated in the parameters and this as no END(FEND) instruction.	Write END in subprogram.
"CAN'T EXECUTE (P)" (Checked at the execution of instruction)	13	131	The device number of pointer (P) or interrupt pointer (I) used as the label added to the destination head is duplicating.	Remove the duplicated number of pointer (P) with the destination head and correct so that the number is not duplicated.
		132	The label of pointer (P) specified by [CJ], [SCJ], [CALL], [CALLP], [JMP], [LEDA/B|FCALL], [LADA/B|BREAK] instructions is not specifide prior to the END instruction.	Read the error step by peripheral device, check the content, and insert destination pointer (P).
		133	(1) Even though the [CALL] instruction is missing, the [RET] instruction has been executed since it is in the program. (2) Even though the [FOR] istruction is missing, the [NEXT] and [LEDA/B|BREAK] instructions have been executed since they are in the program. (3) Since the nesting level for the [CALL], [CALLP] or [FOR] instruction is 6 or deeper, the 6th level nest has been executed. (4) The [RET] or [NEXT] instruction is missing at execution of the [CALL] or [FOR] instruction.	(1) Read the error step by peripheral device, check the content, and correct the program at that step. (2) Nesting level for the [CALL], [CALLP], and [FOR] instructions must be 5 or less.

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CAN'T EXECUTE (P)" (Checked at the execution of instruction)	13	134	Even though subprogram settings are missing, the [CHG] instruction has been executed since it is in the program.	Read the error step by peripheral device and erase the circuit of that [CHG] instruction.
		135	(1) [LEDA/B|IX] to [LEDA|IXEND] instructions are not written as a set. (2) There are more than 32 sets of [LEDA/B|IX] to [LEDA|IXEND] instructions.	(1) Read the error step by peripheral device, check the content, and correct the program at that step. (2) [LEDA/B|IX] to [LEDA|IXEND] instructions must be less than 33 sets.
"CHK FORMAT ERR." Checked at STOP/PAUSE → RUN	* 14	141	Instructions other than LDX, LDIX, ANDX and ANIX (including NOP) are in the circuit block of the [CHK] instruction.	Refer to the content of the detailed error code, and chedk and correct programs related to the [CHK] instruction.
		142	There is more than 1 [CHK] instruction .	
		143	The number of contact points in the circuit block of the [CHK] instruction exceeds 150.	
		144	The [LEDA|CHK] and [LEDA|CHKEND] instructions are not written as a set, or there are 2 or more sets.	
		145	The format of the block shown below preceding the circuit block of the [CHK] instruction is abnormal. 	
		146	The D1 device number of the [CHK|D1|D2] instruction does not match the contact device number preceking the [CJP] instruction.	
		147	There is a place where index qualification is made in the check pattern circuit.	
		148	(1) There is more than 1 check pattern circuit of [LEDA|CHK] to [LEDA|CHKEND] instructions. (2) There are 7 or more check condition circuits in [LEDA|CHK] to [LEDA|CHKEND] instructions. (3) The check condision circuit in [LEDA|CHK] to [LEDA|CHKEND] instructions have been created by instructions other than X and Y contact instructions and comparison instructions. (4) The check pattern circuit of [LEDA|CHK] to [LEDA|CHKEND] instructions has been created by 257 or more steps.	

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CAN'T EXECUTE (1)" (Checked at the occurrence of interruption)	*15	151	The [IRET] instruction exists outside the interrupt program and has been executed.	Read the error step by peripheral device and erase the [IRET] instruction.
		152	No [IRET] instruction in the interrupt program.	Check and correct use of [IRET] instruction inside or outside interrupt program.
		153	An interrupt module is being used though there is no corresponding interrupt pointer (I). At error occurrence, pointer (I) is stored in D9011.	Monitor special register D9011 by peripheral device, check whether or not there is an interrupt program corresponding to the stored numeric values or whether or not the same number exists for the interrupt pointer (I) , and correct.
"CASSETTE ERROR"	*16	-	The memory cassette is not loaded.	Turn the PC power supply OFF, and load the memory cassette.
"RAM ERROR" (Checked at power-on)	*20	201	Error of the CPU sequence program storage RAM	Possible hardware fault, consult your nearest Mitsubishi representative with details.
		202	Error of the CPU work area RAM	
		203	CPU device memory error	
		204	CPU address RAM error	
"OPE. CIRCUIT ERR." (Checked at power-on)	*21	211	The operation circuit executing index qualification in the CPU is not operating normally.	Possible hardware fault, consult your nearest Mitsubishi representative with details.
		212	The CPU hardware (logic) is not operating normally.	
		213	The operation circuit executing PC sequence program in the CPU is not operating normally.	
"WDT ERROR" (Checked at the execution of END instruction)	22	-	Scan time exceeds watchdog error monitor time. (1) User program scan time has in creased. (2) Momentary power failure during program scan has caused apparent scan time to increase.	(1) Check PC program scan time and reduce using the [CJ] instruction. (2) Check for momentary power failures by monitoring special register D9005.
"END NOT EXECUTE" (Checked at end of program)	24	241	The entire stored program has been executed without executing the END instruction. (1) The END instruction has been missed (e.g. memory cassette removed during program execution). (2) The END instruction has been corrupted.	(1) Reset CPU. If error persists, possible hard ware fault, consult your nearest Mitsubishi representative with details.
"MAIN CPU DOWN"	26	-	The main CPU is malfunctioning or broken.	Possible hardware fault, consult your nearest Mitsubishi representative with details.
"UNIT VERIFY ERR." (Checked continuously)	*31	-	Verified data is different from the I/O data at power on. (1) An I/O module (including special function module) has been removed form the base unit while the base unit while the P.C. power is switched on. Or, wrong module is loaded.	Read the detailed error code by peripheral device, check and replace the module corresponding to that numeric value (I/O head number) or monitor special registers D9116 to D9123 by peripheral device, check and replace the module where that data bit is "1".

Error Massage	Error Code (D9008)	Detailed Error Code (F9091)	Error and Cause	Corrective Action
"FUSE BREAK OFF" (Checked continuously)	32	-	Output unit fuse blown.	(1) Check the fuse blown LED indicator of the output module and replace the fuse of the lit module. (2) Read the detailed error code by peripheral device and replace the fuse of the fuse of the output module corresponding to that numeric value (I/O head number), or monitor special registers D9100 to D9107 by peripheral device and replace the fuse of the output module where that data bit is "1".
"CONTROL-BUS ERR."	40	401	Incorrect FROM/TO instruction execution.	Hardware fault (CPU, special function unit and/or base unit). Consult your nearest Mitsubishi representative with details.
		402	During paramerer I/O assignment, special function modules cannot be accessed at initial communication. At error occurrence, the head I/O number (the upper 2 digits of a 3-degit expression) of the special function module causing the error is stored in D9011.	
"SP. UNIT DOWN"	41	411	No response from special function unit after execution of FROM/TO instruction.	Hardware error of the accessed special function module. Consult your nearest Mitsubishi representative with details.
		412	During parameter I/O assignmert, at initial communication, responses from special function modules have not been returned. At error occurrence, the head I/O number (the upper 2 digits of a 3-diget expression) of the special function module causing the error is stored in D9011.	
"LINK UNIT ERROR"	*42	-	AJ71R22 or AJ71P22 located in master station.	Remove AJ71R22 or AJ71P22 from master station.
"I/O INT. ERROR"	*43	-	Interrupt signal received with no interrupt module present.	Since a hardware error has occurred in one of the modules, replace the modules one by one to find the faulty module. Consult your nearest Mitsubishi representative with details.
"SP. UNIT LAY. ERR."	*44	441	I/O modules allocated in parameter settings by peripheral device have been allocated by special function modules. Or, the opposite settings have been executed.	Reset I/O assignments in parameters by peripheral device according to the loading status of the special function modules.
		442	More than 8 special function modules [except for the AI61(S1)] which can start interrupts to the CPU have been executed.	Load less than 9 special function modules [except for the AI61(S1)] which can start interrupts to the CPU.
		443	More than 1 AJ71P22 or 1 A71R22 has been loaded.	Load less than 2 AJ71P22s or 2 AJ71R22s.

Error Massage	Error Code (D9008)	Detailed Error Code (F9091)	Error and Cause	Corrective Action
"SP. UNIT LAY. ERR."	*44	444	More than 6 computer link modules, etc., have been loaded to 1 CPU module.	Load less than 7 computer link modules.
		445	More than AI61(S1) has been loaded.	Load only 1 AI61.
		446	The modules of MNETMINI automatic refresh allocated in parameter settings by peripheral device and the names of the modules of actually linked station numbers are incorrect.	Reset the module assignments of the MNETMINI automatic refresh in parameter settings by perpheral device according to the modules of station numbers actually linked.
		447	The number special function modules which can use dedicated instructions, registered by I/O assignment per one CPU module (number of modules to be loaded) is larger than the specified limit. (The total of computers shown below is 1344 or more.) (Number of loaded AD59 X 5) (Number of loaded AD57(S1/AD58 X 8) (Number of loaded AJ71C24(S3) X 10) (Number of loaded AJ71C21(S1) X 29) + (Number of loaded AJ71PT32(S3) X 125) Total >1344	Decrease the number of loaded special function modules.
"SP. UNIT ERROR" (Checked when FROM/T0 instruction, or special function module dedicated instruction is specified.)	46	461	There is no special function module in the area specified by the FROM/TO instruction.	Read the error step by peripheral device, check and correct the content of the FROM/TO instruction of that step.
		462	There is no special function module in the area specified by the FROM/TO instruction or there is no corresponding special function module.	Read the error step by peripheral device, check and correct the content of the special function module dedicated instruction of that step.
"LINK PARA. ERROR"	*47	-	(1) The link range is set in parameter settings by peripheral device, and for some reason, the content written to the link parameter area differs from the link parameter content read by the CPU. (2) 0 slave stations set.	(1) Re-Write link parameters form peripheral programming unit to PC. (2) Persistent error occurrence may indicated hardware fault. Consult your nearest Mitsubishi representative with details.
"OPERATION ERROR" (Checked during execution of instruction)	50	501	(1) When using file register (R), operations have been executed exceeding the specified range for the device number and block number of file register (R). (2) The file register is used in the program without executing file register capacity settings.	Read the error step by peripheral device, check and correct the program of that step.
		502	The combination of devices specified by instruction is incorrect.	

Error Massage	Error Code (D9008)	Detailed Error Code (F9091)	Error and Cause	Corrective Action
"OPERATION ERROR" (Checked during execution of instruction)	50	503	The storage data of specified devices or the constants are not within the usable range.	Read the error step by peripheral device, check and correct the program of that step.
		504	The quantity of settings used for handled data has exceeded the usable range.	
		505	(1) The station number specified by instruction [LEDA/B|LREP], [LEDA/B|LWTP], [LRDP] or [LWTP] is not a local station. (2) The head I/O number specified by instruction [LEDA/B|RFRP], [LEDA/B|RTOP], [RFRP] or [RTOP] is not a remote station.	
		506	The head I/O number specified by instruction [LEDA/B|RFRP], [LEDA/B|RTOP], [RFRP] or [RTOP] is not a special function module.	
		507	(1) While the AD57 (S1) or the AD58 is executiong instructions by partial procedding, other instructions have been output to the same module. (2) While the AD57 (S1) or the AD58 is executing instructiuons by partial processing, instructions have been output to other AD57 (S1) or AD58 by partial processing.	Read the error step by peripheral device and provide interlock by special relay M9066 or change the program structure and correct. This prevents the execution of other instructions to the same module while executing instructions to the AD57 (S1) or AD58 by partial processing and prevents the execution of instructions to other AD57 (S1) or AD58 by partial processing.
		509	(1) An instruction which cannot be executed by remote terminal module connected to the MNETMINI-S3 was executed to the modules. (2) When the [PRC] instruction was executed to a remote terminal, the communication request registration areas overflowed. (3) The [PIDCONT] instruction was executed without executing the [PIDINIT] or [PIDCONT] instruction. The [PID57] instruction was executed without executing the [PIDINIT] or [PIDCONT] instruction.	(1) Read the error step by peripheral device and correct the program, meeting loaded conditions of remote terminal module. (2) Provide interlock using M9081 (communication request registration areas BUSY signal) or D9081 (number of vacant areas in the communication is executed to a remote terminal. (3) Execute the [PIDCONT] instruction after execution of the [PIDINIT] instruction. Execute the [PID57] instruction after execution of the [PIDINIT] and [PIDCONT] instructions.
"MAIN CPU DOWN"	60		(1) INT instruction processed in microcomputer program area. (2) CPU malfunction due to noise. (3) Hardware fault.	(1) Remove INT (2) Eliminate noise. (3) Hardware fault
"BATTERY ERROR" (Checked at power-on)	70		(1) Battery voltage low. (2) Battery not connected.	(1) Replace the battery. (2) When using RAM memory or the power failure compensation function, load connectors.

1.3.3 Self-diagnosis

When an error occurs in the PC RUN state, the CPU is stopped by using self-diagnosis, and the error is displayed. Error contents are shown in the following table. The following error code list explains the processing methods for error cancellation.

Self-Diagnosis List

Dianosis		CPU Status	"RUN" LED Status	Error Indication Contents		Applicable CPU Model Name			
				A1 and A2CPU ERROR LED Displays	LED Display Message (A3(A)CPU only)	A0J	A1	A2	A3
Memory error	Instruction code check	Stop	☆ Flicker	ON	INSTRCT. CODE ERR	O	O	O	O
	Parameter setting check			ON	PARAMETER ERROR	-	O	O	O
	No END instruction			ON	MISSING END INS.	O	O	O	O
	Instruction execution disable			ON	CAN'T EXECUTE	O	O	O	O
	Format (CHK instruction) check			ON	CHK FORMAT ERR.	-	O	O	O
	Instruction execution disable			ON	CAN'T EXECUTE (I)	-	O	O	O
	No memory cassette			ON	CASSETTE ERROR	-	-	O	O
CPU error	RAM check	Stop	☆ Flicker	ON	RAM ERROR	-	O	O	O
	Operation circuit check			ON	OPE. CIRCUIT ERR.	-	O	O	O
	Watchdog error check			ON	WDT ERROR	O	O	O	O
	Sub CPU check			-	SUB-CPU ERROR	-	-	-	O
	END instruction unexecution			ON	END NOT EXECUTE	O	O	O	O
	Endless loop execution, MAIN CPU malfunction			-	WDT ERROR	-	-	-	O
I/O error	I/O module verify	Stop / Run	☆ Flicker / On	ON	UNIT VERIFY ERR.	-	O	O	O
	Fuse blow			ON	FUSE BREAK OFF	O	O	O	O
Special function module error	Control bus check	Stop	☆ Flicker	ON	CONTROL-BUS ERR.	O	O	O	O
	Special function unit error			ON	SP. UNIT DOWN	O	O	O	O
	Link module error			ON	LINK UNIT ERROR	-	O	O	O
	I/O interruption error			ON	I/O INT. ERROR	-	O	O	O
	Special function module assignment			ON	SP. UNIT LAY. ERR.	-	O	O	O

Dianosis		CPU Status	"RUN" LED Status	Error Indication Contents		Applicable CPU Model Name			
				A1 and A2CPU ERROR LED Displays	LED Display Message (A3(A)CPU only)	A0J	A1	A2	A3
Special function module error	Special function module error	Stop/Run	☆Flicker/On	ON	SP.UNIT ERROR	O	O	O	O
	Link parameter error	Run	On	ON	LINK PARA. ERROR	-	O	O	O
Battery error	Battery low	Run	On	ON	BATTERY ERROR	O	O	O	O
* Operation check error		Stop/Run	☆Flicker/On	ON	OPERATION ERROR	O	O	O	O
MAIN CPU malfunction		Stop	Flicker	-	MAIN-CPU DOWN	-	-	-	O

REMARKS

1. When two types of contents are described in the CPU state and the RUN LED state area, the setting can be changed by using a peripheral device (GPP).
2. When the error contents of an instruction are CHK in a *symbol operation check error, the LED display message is as follows:
   <CHK> ERROR [ ][ ][ ]
   ↑——Displays the 3-digit faulty number.
3. ☆Shows OFF when an A3CPU is used.

1.3.4 Judging the quality of a CPU

The quality of a PC CPU can be judged by turning ON the power supply under the normal start conditions of a sequence program.
Write the END instruction to step 0 of the sequence program.
If RUN LED is ON when the CPU is set to RUN, the CPU qualitey is acceptable.

(1) Operations by using an A6GPP

1) Paramerers and programs are read by using the following operation from the CPU to the A6GPP.
Key operations

[PC] [RD] ■Parameter + main [GO] [GO]

2) Write the END instruction to step 0.
However, when the CPU quality is acceptable and programs do not need changing, write down step 0 of the list program (or insert an END instruction).

[LST] [RD] [SSN] [0] [GO] Step 0 is read.

[WR] [END] [GO] END is written to step 0.

3) Set the CPU to STOP, and write this program to the CPU.

[PC] [WR] ■Parameter + main [GO] [GO]

[Writing step 0 of the main program is sufficient.]

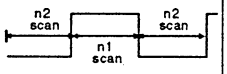
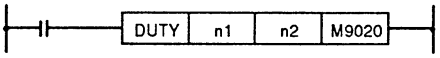
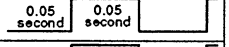
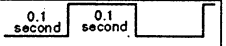
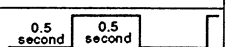
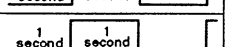
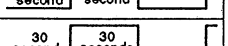
4) Set the CPU to RESET.

5) Set the CPU to RUN.
When the RUN LED is ON, the CPU quality is acceptable.
If the RUN LED is OFF or flickers, the CPU is quality is not acceptable.

6) If the CPU quality is acceptable, return the program of step 0 that was written down to the original program , and write it to the CPU.

1.3.5 Special relay M

Special relays are internal relays of which applications have been determined inside the PC. Therefore, do not turn ON/OFF the special relays on the program (Except the ones with numbers marked *1 and *2 in the table). Application acceptability varies according to the type of CPU.

Number	Name	Description	Details	Applicable CPU
*1 M9000	Fuse blown	OFF : Normal ON : Fuse blown unit	• Turned on when there is one or more output modules of which fuse has been blown. Remains ON even if normal status is restored.	All CPUs
*1 M9002	I/O module verify error	OFF : Normal ON : Error	• Turned on if the status of I/O module is different from entered status when power is turned on. Remains ON even if normal status is restored.	
*1 M9004	MINI link master module error	OFF : Normal ON : Error	• Turned on when a MINI(S3) link error is detected in the installed AJ71PT32(S3). Remains ON even when the normal status is restored.	AnACPU-F
*1 M9005	AC DOWN detection	OFF : AC power good ON : AC power DOWN	• Turned ON when an momentary power failure of 20 msec or less occurred. Reset when POWER switch is moved from OFF to ON position.	All CPUs
M9006	Battery low	OFF : Normal ON : Battery low	• Turned ON when battery voltage reduces to less than specified. Turned OFF when battery voltage becomes normal.	
*1 M9007	Battery low latch	OFF : Normal ON : Battery low	• Turned ON when battery voltage reduces to less than specified. Remains ON even if battery voltage becomes normal.	
*1 M9008	Self-diagnostic error	OFF : No error ON : Error	• Turned ON when error is found as a result of self-diagnosis.	
M9009	Annunciator detection	OFF : No detection ON : Detected	• Turned ON when [OUT F] or [SET F] instruction is executed. Switched OFF when D9124 data is zeroed.	
M9010	Operation error flag	OFF : No error ON : Error	• Turned ON when operation error occurs during execution of application instruction. Turned OFF when error is eliminated.	Except for AnACPU-F
*1 M9011	Operation error flag	OFF : No error ON : Error	• Turned ON when operation error occurs during execution of application instruction. Remains ON even if normal status is restored.	All CPUs
M9012	Carry flag	OFF : Carry off ON : Carry on	• Carry flag used in application instruction.	
M9016	Data memory clear flag	OFF : No processing ON : Output clear	• Clears the data memory including the latch range (other than special relays and special registers) in remote run mode from computer, etc. when M9016 is ON.	
M9017	Data memory clear flag	OFF : No processing ON : Output clear	• Clears the unlatched data memory (other than special relays and special registers) in remote run mode from computer, etc. when M9017 is ON.	
M9020	User timing clock No. 0		• Relay which repeats ON/OFF at intervals of predetermined scan. • When power is turned on or reset is performed, the clock starts with off. • Set the intervals of ON/OFF by [DUTY] instruction. 	
M9021	User timing clock No. 1			
M9022	User timing clock No. 2			
M9023	User timing clock No. 3			
M9024	User timing clock No. 4			
*2 M9025	Clock data set request	OFF : No processing ON : Set requested	• Writes clock data from D9025 to D9028 to the clock element after the [END] instruction is executed during the scan in which M9025 has changed from OFF to ON.	Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU
M9026	Clock data error	OFF : No error ON : Error	• Switched ON by clock data (D9025 to D9028) error.	
M9027	Clock data display	OFF : No processing ON : Display	• Clock data is read from D9025 to D9028 and indicated on the CPU front LED display.	A3NCPU-F and A3ACPU-F
*2 M9028	Clock data read request	OFF : No processing ON : Read request	• Reads clock data to D9025 to D9028 in BCD when M9028 is ON.	Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU
M9030	0.1 second clock		• 0.1 second, 0.2 second, 1 second, 2 seconds, and 1 minute clocks are generated. • Not turned ON and OFF per scan but turned ON and OFF even during scan if corresponding time has elapsed. • Starts with OFF when power is turned ON or reset is performed.	All CPUs
M9031	0.2 second clock			
M9032	1 second clock			
M9033	2 second clock			
M9034	1 minute clock			

Number	Name	Description	Details	Applicable CPU
M9036	Normally ON	ON OFF	• Used as dummy contacts of initialization and application instruction in sequence program. • M9036 and M9037 are turned ON and OFF without regard to position of key switch on CPU front. M9038 and M9039 are under the same condition as RN status except when the key switch is at STOP position, and turned off and on. Switched OFF if the key switch is in STOP position. M9038 is ON for one scan only and M9039 is OFF for one scan only if the key switch is not in STOP position.	All CPUs
M9037	Normally OFF	ON OFF		
M9038	ON only for 1 scan after RUN	ON OFF 1 scan		
M9039	RUN flag (OFF only for 1 scan after RUN)	ON OFF 1 scan		
M9040	PAUSE enable coil	OFF : PAUSE disabled ON : PAUSE enabled	• When RUN key switch is at PAUSE position or remote pause contact has turned ON and if M9040 is ON, PAUSE mode is set and M9041 is turned ON.	
M9041	PAUSE status contact	OFF : Not during pause ON : During pause		
M9042	Stop status contact	OFF : Not during stop ON : During stop	• Switched ON when the RUN key switch is in STOP position.	
M9043	Sampling trace completion	OFF : During sampling trace ON : Sampling trace completion	• Turned ON upon completion of sampling trace performed the number of times preset by parameter after [STRA] instruction is executed. Reset when [STRAR] instruction is executed.	
M9044	Sampling trace	0→1 The same as [STRA] 1→0 The same as [STRAR]	• Turning M9044 ON/OFF allows pseudo-execution of [STRA] and [STRAR] instructions. (M9044 is turned ON/OFF forcibly by peripheral devices.) When M9044 is turned from OFF to ON: [STRA] instruction When M9044 is turned from ON to OFF: [STRAR] instruction At this time, a value stored in D9044 is used for a condition of sampling trace. (When scan, when time → time (in unit of 10 msec)	Except for A1SCPU
M9046	Sampling trace	OFF : Except during trace ON : During trace	• Switched ON during sampling trace.	All CPUs
M9047	Sampling trace preparration	OFF : Sampling trace stop ON : Sampling trace start	• Turn M9047 ON to start sampling trace. Turn it OFF to stop sampling trace.	
*2 M9048	RUN LED flash flag	ON : Flashes when the annunciator is turned on OFF : Does not flash when the annunciator is turned on	• Sets whether the RUN LED flashes when the annunciator relay F[ ] is turned on by an A0J2HCPU.	A0J2HCPU
M9049	Switching the number of output characters	OFF : Up to NULL code are output ON : 16 characters are output	• When M9049 is off, up to NULL (00H) code are output. When M9049 is on, ASCII codes of 16 characters are output.	Except for A2CCPU and A2CCPUC24(PRF)
M9051	[CHG] instruction execution disable	OFF : Disable ON : Enable	• Switched ON to disable the [CHG] instruction. Switched ON when program transfer is requested and automatically switched OFF when transfer is complete.	A3NCPU-F and A3ACPU-F
*2 M9052	[SEG] instruction switching	OFF : 7SEG display ON : I/O partial refresh	• Switched ON to execute the [SEG] instruction as an I/O partial refresh instruction. Switched OFF to execute the [SEG] instruction as a 7SEG display instruction.	All CPUs
*2 M9053	[EI]/[DI] instruction switching	OFF : Sequence interrupt control ON : Link interrupt control	• Switched ON to execute the link refresh enable, disable (EI, DI) instructions.	Except for AnACPU-F
M9054	STEP RUN flag	OFF : Other than step RUN ON : During step RUN	• Switched ON when the RUN key switch is in STEP RUN position.	Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU
M9055	Status latch complete flag	OFF : Not complete ON : Complete	• Turned ON when status latch is completed. Turned OFF by reset instruction.	All CPUs
M9056	Main program P, I set request	ON : P, I set request OFF : Other than P, I set request	• Provides P, I set request after transfer of the other program (for example, subprogram when main program is being RUN) is complete during RUN. Automatically switched OFF when P, I setting is complete.	A3NCPU-F and A3ACPU-F
M9057	Subprogram P, I set request	ON : P, I set request OFF : Other than P.I set request		
M9060	Remote terminal error	OFF : Normal ON : Error	• Turned ON when one of remote terminal modules has become a faulty station. (Communication error is detected when normal communication is not restored after the number of retries set at D9174) • Turned OFF when communication with all remote terminal modules is restored to normal with automatic online return enabled. • Remains ON when automatic online return is disabled. • Not turned ON or OFF when communication is suspended at error detection.	A2CCPU and A2CCPUC24(PRF)

Number	Name	Description	Details	Applicable CPU
M9061	Communication error	OFF : Normal ON : Error	• Turned ON when communication with a remote terminal module or an I/O module is faulty. Communication error occurs due to the following reasons. • Initial data error • Cable breakage • Power off for remote terminal modules or I/O modules • Turned OFF when communication is restored to normal with automatic online return enabled. • Remains ON when communication is suspended at error detection with automatic online return disabled.	A2CCPU and A2CCPUC24(PRF)
M9065	Divide transfer state	OFF : Except during divide processing ON : During divide processing	• In the processing with an AD57(S1)/AD58, turned ON when executing a canvas screen transfer by divice processing and turned OFF when divide processing has been completed.	AnACPU-F
*2 M9066	Transfer processing switching	OFF : Batch transmisison ON : Divide transmission	• In the processing with an AD57(S1)/AD58, turned ON when executing a canvas screen transfer by divide procesisng .	
M9067	I/O module error detection	OFF : Normal ON : Error	• Turned ON when one of I/O modules has become a faulty station. (Communication error occurs when normal communication is not restored after the number of retries set at D9174) • Turned OFF when communication with all I/O modules is restored to normal with automatic online return enabled. • Remains ON when automatic online return is disabled. • Not turned ON or OFF when communication is suspended at error detection.	A2CCPU and A2CCPUC24(PRF)
M9068	Test mode	OFF : Automatic online return enabled : Automatic online return disabled : Communication suspended at online error ON : Line check	• Turned ON when line check with I/O modules and remote terminal modules is performed. • If turned OFF, communication with I/O modules and remote terminal modules is performed.	A2CCPU
M9069	Output at line error	OFF : All outputs are turned off ON : Outputs are retained	• Sets whether all outputs are turned off or retained at communication error • OFF ... All outputs are turned off at communication error. • ON ..... Outputs before communication error are retained.	A2CCPU and A2CCPUC24(PRF)
M9073	Clock data set request	OFF : No processing ON : Set requested	• Writes clock data from D9073 to D9076 to the clock element after the END instruction is executed during the scan in which M9073 has been switched from OFF to ON.	A2CCPUC24(PRF)
M9074	Clock data error	OFF : No error ON : Error	• Turned ON when there is a clock data (M9073 to D7076) error. Turned OFF when there is no error.	
M9076	Clock data read request	OFF : No processing ON : Read request	• When M9076 is ON, clock data is read from D9073 to D9076 at the BCD value.	
M9081	Communication request to remote terminal modules	OFF : Communication request to remote terminal modules enabled ON : Communication request to remote terminal modules disabled	• Indication of communication enable/disable to remote terminal modules connected to the AJ71PT32-S3 or A2CCPU.	AnACPU-F, A2CCPU and A2CCPUC24(PRF)
M9082	Final station number disagreement	OFF : Final station number agreement ON : Final station number disagreement	• Turned ON when the final station number of the remote terminal modules and remote I/O modules connected to the A2CCPU disagrees with the total number of stations set in the initial setting. • Turned OFF when the final station number agrees with the total number of stations at STOP→RUN.	A2CCPU and A2CCPUC24(PRF)
*2 M9084	Error check	OFF : Checks enabled ON : Checks disabled	• Specify whether the following errors are to be checked or not after the [END] instruction is executed (to reduce END processing time): • Fuse blown • I/O unit verify error • Battery error	Except for A2CCPU and A2CCPUC24(PRF)
*2 M9089	ERR terminal output	OFF : ERR terminal OFF ON : ERR terminal ON	• Turned ON when output from "ERR terminal" in the sequence program. • Turned OFF when both M9089 and M9090 are turned OFF.	A2CCPU and A2CCPUC24(PRF)
M9090	ERR terminal output	OFF : ERR terminal OFF ON : ERR terminal ON	• Turned ON when MINI-S3 link error or sequence program error (when operation is stopped) occurs. • Turned OFF when MINI-S3 link and sequence program is restored to normal.	
M9091	Operations error Detail flag	OFF : No Error ON : Error	• Turned on when an operations error detail factor is stored to D9091. Remains on even when the normal status is restored.	AnACPU-F
M9091	Microcomputer subroutine call error flag	OFF : No error ON : Error	• Turned ON when an error occurs while executing a microcomputer package. Ramains ON even when the normal status is restored.	Except for AnACPU-F

Number	Name	Description	Details	Applicable CPU
*2 *3 M9094	I/O change flag	OFF : Changed ON : Not changed	• After the head address of the required I/O module is set to D9094, switching M9094 ON allows the I/O module to be changed in online mode. (One module is only allowed to be changed by one setting.) • To be switched ON in the program or peripheral device test mode to change the module during CPU RUN. To be switched ON in peripheral device test mode to change the module during CPU STOP. • RUN/STOP mode must not be changed until I/O module change is complete.	Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU
M9100	SFC program registration	OFF : No SFC program ON : SFC program registered	• Turned ON if the SFC program is registered, and turned OFF if it is not.	All CPUs
*2 M9101	SFC program start/stop	OFF : SFC program stop ON : SFC program start	• Should be turned ON by the program if the SFC program is to be started. If turned OFF, operation output of the execution step is turned OFF and the SFC program is stopped.	
*2 M9102	SFC program starting status	OFF : Initial start ON : Continuous start	• Selects the starting step when the SFC program is restarted using M9101. OFF : All execution conditions when the SFC program stopped are cleared, and the program is started with the initial step of block 0. ON : Started with the step of the block being executed when the program stopped.	
*2 M9103	Consecutive step transfer enable/disable	OFF : Consecutive step transfer disable ON : Consecutive step transfer enable	• Selects consecutive or step-by-step transfer of steps of which transitions are established when all of the transitions of consecutive steps are established. ON : Consecutive transfer is executed (Consecutive transfer enable) OFF: One step per one scan is transferred (Consecutive transfer disable)	
M9104	Consecutive transfer prevention flag	OFF : Transfer complete ON : Transfer incomplete	• Set when consecutive transfer is not executed with consecutive transfer enabled. Reset when transfer of one step is completed. Consecutive transfer of a step can be prevented by writing an AND condition to corresponding M9104.	
*2 M9108	Step transfer monitoring timer start (corresponds to D9108)	OFF : Monitoring timer reset ON : Monitoring timer start	• Turned ON when the step transfer monitoring timer is started. • Turned OFF when the monitoring timer is reset.	
*2 M9109	Step transfer monitoring timer start (corresponds to D9109)			
*2 M9110	Step transfer monitoring timer start (corresponds to D9110)			
*2 M9111	Step transfer monitoring timer start (corresponds to D9111)			
*2 M9112	Step transfer monitoring timer start (corresponds to D9112)			
*2 M9113	Step transfer monitoring timer start (corresponds to D9113)			
*2 M9114	Step transfer monitoring timer start (corresponds to D9114)			
M9180	Active step sampling trace complete flag	OFF : Trace start ON : Trace complete	• Set when sampling trace of all specified blocks is completed. Reset when sampling trace is started.	
M9181	Active step sampling trace execution flag	OFF : Trace not executed ON : Trace being executed	• Set when sampling trace is being executed. Reset when sampling trace is completed or suspended.	
*2 M9182	Active step sampling trace enable	OFF : Trace disable/suspend ON : Trace enable	• Selects sampling trace execution enable/disable. ON : Sampling trace execution is enabled. OFF: Sampling trace execution is disabled. if turned off during sampling trace execution, trace is suspended..	

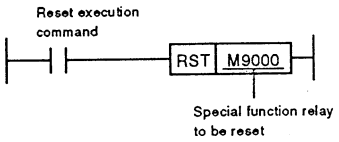
Number	Name	Description	Details	Applicable CPU
M9196	Operation output at block stop	OFF : Coil output off ON : Coil output on	• Selects the operation output when block stop is executed. ON : Retains the ON/OFF status of the coil being used by using operation output of the step being executed at block stop. OFF: All coil outputs are turned off. (Operation output by the SET instruction is retained regardless of the ON/OFF status of M9196.)	All CPUs

POINTS

(1) Contents of the M special relays are all cleared by power OFF, latch clear or reset with the reset key switch. When the RUN key switch is set in the STOP position, the contents are retained.

(2) The above relays with numbers marked *1 remain ON if normal status is restored. Therefore, to turn them OFF, use the following method.

1) Method by user program
Insert the circuit shown at the right into the program and turn ON the reset execution command contact to clear the special relay M.



2) Method using peripheral devices
Perform forced reset by use of the test function of peripheral devices. For the operation procedure, refer to the manuals for peripheral devices.

3) By moving the RESET key switch on the CPU front to the RESET position, the special relays are turned OFF.

(3) Special relays marked *2 above are switched ON/OFF in the sequence program.

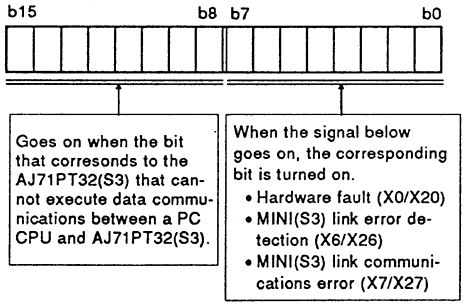
(4) Special relays marked *3 above are switched ON/OFF in test mode of the peripheral device.

(5) Special relays marked *4 above are reset only when the power is turned from OFF to ON.

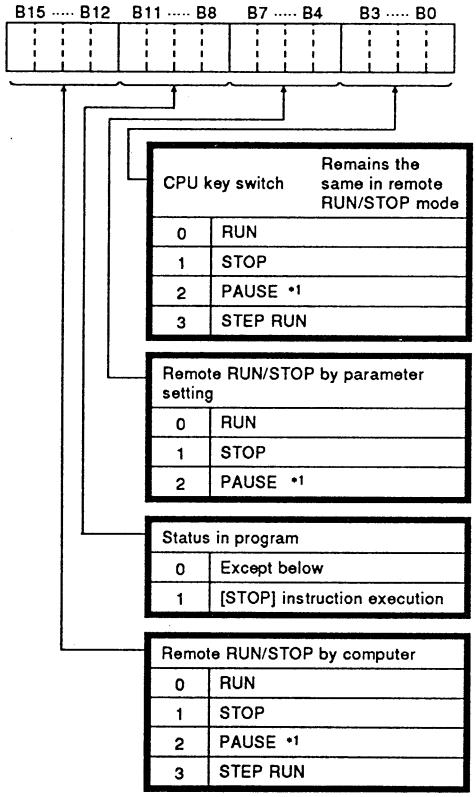
(6) Since M9102 is latched automatically, even if the power supply goes off, M9102 maintains its ON/OFF state.

1.3.6 Special register D

Special registers are data registers of which applications have been determined inside the PC. Therefore, do not write data to the special registers in the program (except the ones with numbers marked *2 in the table).

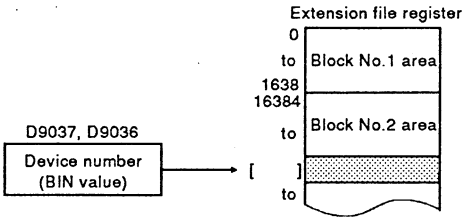
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>D9000</td><td>Fuse blown</td><td>Fuse blown module number</td><td>• When fuse blown modules are detected, the lowest number of detected modules is stored in hexadecimal. (Example: When fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) To monitor the number by peripheral devices, perform monitor operation given in hexadecimal.
(Cleared when all contents of D9100 to D9107 are reset to 0)</td><td>Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU</td></tr>
<tr><td>D9001</td><td>Fuse blown</td><td>Fuse blown module number</td><td>• Stores the module numbers corresponding to setting switch numbers or base slot numbers when fuse blow occurred.
<table>
<tr><th colspan="2">I/O module for A0J2</th><th colspan="2">Extension base unit</th></tr>
<tr><th>Setting switch</th><th>Stored data</th><th>Base unit slot No.</th><th>Stored data</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>2</td><td>1</td><td>6</td></tr>
<tr><td>2</td><td>3</td><td>2</td><td>7</td></tr>
<tr><td>3</td><td>4</td><td>3</td><td>8</td></tr>
<tr><td>4</td><td>5</td><td></td><td></td></tr>
<tr><td>5</td><td>6</td><td></td><td></td></tr>
<tr><td>6</td><td>7</td><td></td><td></td></tr>
<tr><td>7</td><td>8</td><td></td><td></td></tr>
</table></td><td>A0J2HCPU</td></tr>
<tr><td rowspan="2">D9002</td><td rowspan="2">I/O module verify error</td><td rowspan="2">I/O module verify error module number</td><td>• If I/O modules, of which data are different from data entered, are detected when the power is turned on, the first I/O number of the lowest number module among the detected modules is stored in hexadecimal. (Storing method is the same as that of D9000) To monitor the number by peripheral devices, perform monitor operation given in hexadecimal.
(Cleared when all contents of D9116 to D9123 are reset to 0)
• The I/O module of a remote I/O station is also verified.</td><td>Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU</td></tr>
<tr><td>• Stores the number that corresponds to the setting switch number or base unit number when an I/O module is detected that is different from the registered I/O module information when the power supply was turned on. (The storing method is the same as that of the D9001.)
• In the case of a remote I/O module, (module I/O number/10H) + 1 is stored.</td><td rowspan="2">A0J2HCPU</td></tr>
<tr><td>D9003</td><td>SUM instruction detection bits</td><td>The number of bits detected by SUM instruction detection</td><td>• The number of bits detected by execution of the SUM instruction are stored in BIN code and updated every execution thereafter.</td></tr>
<tr><td>D9004</td><td>MINI link master module error</td><td>Error detection status</td><td>• Stores the error detection status of the MINI(S3) link to the installed AJ71PT32(S3).

</td><td>AnACPU-F</td></tr>
<tr><td>D9005</td><td>AC DOWN counter</td><td>AC DOWN count</td><td>• 1 is added each time input voltage becomes 80% or less of rating while the CPU unit is performing operation, and the value is stored in BIN code.</td><td rowspan="2">All CPUs</td></tr>
<tr><td>D9008</td><td>Self-diagnostic error</td><td>Self-diagnostic error number</td><td>• When error is found as a result of self-diagnosis, error number is stored in BIN code.</td></tr>
</table>

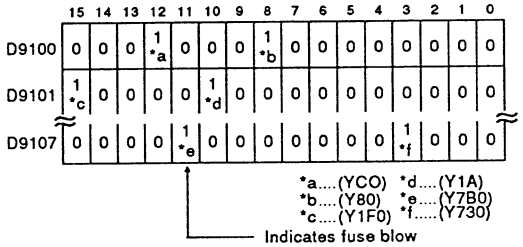
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>D9009</td><td>Annunciator detection</td><td>F number at which external failure has occurred</td><td>• When one of F0 to 255 is turned ON by [OUT F] or [SET F], the F number, which has been detected earliest among the F numbers which have turned ON, is stored in BIN code.
• D9009 can be cleared by executing [RST F] or [LEDR] instruction. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.

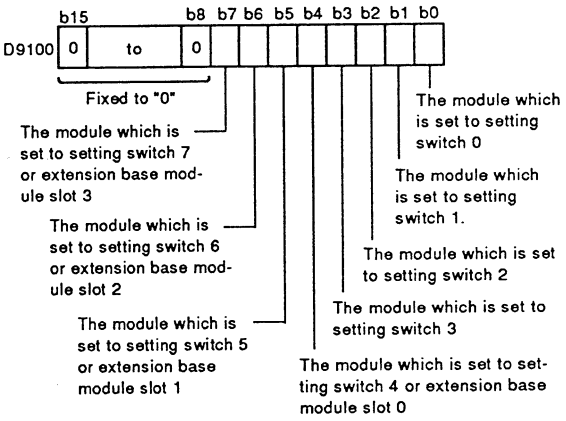
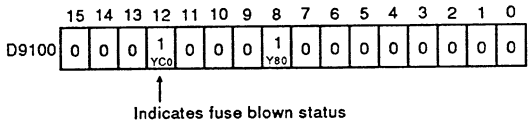
• When one of F0 to 255 is turned ON by [OUT F] or [SET F], the F number, which has been detected earliest among the F numbers which have turned ON, is stored in BIN code.
• D9009 can be cleared by executing [RST F] or [LEDR] instruction or moving INDICATOR RESET switch on CPU front to ON position. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.</td><td rowspan="6">All CPUs</td></tr>
<tr><td>D9010</td><td>Error step</td><td>Step number at which operation error has occurred</td><td>• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Thereafter, each time operation error occurs, the contents of D9010 are updated.</td></tr>
<tr><td>D9011</td><td>Error step</td><td>Step number at which operation error has occurred</td><td>• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Since storage into D9011 is made when M9011 changes from OFF to ON, the contents of D9011 cannot be updated unless M9011 is cleared by user program.</td></tr>
<tr><td>D9014</td><td>I/O control mode</td><td>I/O control mode number</td><td>• The I/O control mode set is returned in any of the following numbers:
0. Both input and output in direct mode
1. Input in refresh mode, output in direct mode
3. Both input and output in refresh mode</td></tr>
<tr><td>D9015</td><td>CPU operating states</td><td>Operating states of CPU</td><td>• The operating states of CPU as shown below are stored in D9015.
 

*1: When the CPU is in RUN mode and M9040 is off, the CPU remains in RUN mode if changed to PAUSE mode.</td></tr>
<tr><td>D9016</td><td>Program number</td><td>0 : Main program (ROM)
1 : Main program (RAM)
2 : Subprogram (RAM)</td><td>• Indicates which sequence program is run presently. One value of 0 to 2 is stored in BIN code. (2 is only valid for the A3N-F.)</td></tr>
<tr><td>D9017</td><td>Scan time</td><td>Minimum scan time (per 10 msec)</td><td>• If scan time is smaller than the content of D9017. the value is newly stored at each END. Namely, the minimum value of scan time is stored into D9017 in BIN code.</td></tr>
<tr><td>D9018</td><td>Scan time</td><td>Scan time (per 10 msec)</td><td>• Scan time is stored in BIN code at each END and always rewritten.</td></tr>
</table>

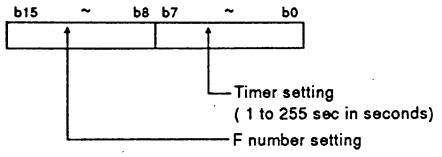
Number	Name	Description	Details	Applicable CPU
D9019	Scan time	Maximum scan time (per 10 msec)	• If scan time is larger than the content of D9019, the value is newly stored at each END. Namely, the maximum value of scan time is stored into D9019 in BIN code.	All CPUs
*2 D9020	Constant scan	Constant scan time Set by use in 10 (msec increments)	• Sets the interval between consecutive program starts in multiples of 10 msec. 0: No setting 1 to 200: Set. Program is executed at intervals of (set value) x 10 msec	
D9021 D9022 D9023 D9024 D9025 D9026 D9027 D9028 D9029 D9030 D9031 D9032 D9033 D9034	Remote terminal parameter setting	1 to 61	• Sets the head station number (1 to 61) of remote terminal modules connected to A2C. Setting is not necessarily in the order of station numbers. D9021 Remote terminal unit No. 1 area D9022 Remote terminal unit No. 2 area D9033 Remote terminal unit No. 13 area D9034 Remote terminal unit No. 14 area	A2CCPU and A2CCPUC24(PRF)
*2 D9025	Clock data	Clock data (Year,month)	• Stores the year (2 lower digits) and month in BCD. B15 ..... B12 B11 ..... B8 B7 ..... B4 B3 ..... B0 Year Month (Example) 1987, July H8707	Except for A2CCPU, A2CCPUC24(PRF) and A0J2HCPU
*2 D9026	Clock data	Clock data (Day,hour)	• Stores the day and hour in BCD. B15 ..... B12 B11 ..... B8 B7 ..... B4 B3 ..... B0 Day Hour (Example) 31st, 10 o'clock H3110	
*2 D9027	Clock data	Clock data (Minute,second)	• Stores the minute and second in BCD. B15 ..... B12 B11 ..... B8 B7 ..... B4 B3 ..... B0 Minute Second (Example) 35 minutes, 48 seconds H3548	
*2 D9028	Clock data	Clock data (Day of the week)	• Stores the day of the week in BCD. 0 must be set (Example) Friday H0005 Day of the week: 0 Sunday, 1 Monday, 2 Tuesday, 3 Wednesday, 4 Thursday, 5 Friday, 6 Saturday	
D9035	Attribute of remote terminal module	0 : Mitsubishi standard protocol 1 : No protocol	• Sets attribute of each remote terminal module connected to A2C with 0 or 1 at each bit. 0: Conforms to the Mitsubishi standard protocol 1: No-protocol mode of AJ35PTF-R2 • Data configuration D9035 b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0 Remote terminal No. 1 Remote terminal No. 2 Remote terminal No. 3 Remote terminal No. 13 Remote terminal No. 14	A2CCPU and A2CCPUC24(PRF)

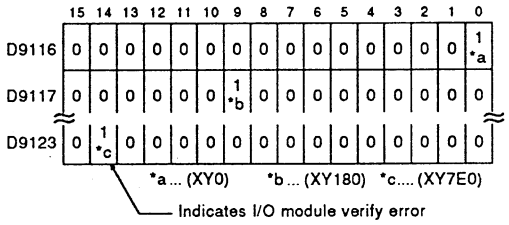
Number	Name	Description	Details	Applicable CPU
D9035	Extension file register	Used block number	• The block number of the currently utilized extension file register is stored in BIN code.	AnACPU-F
D9036	Total number of stations	1 to 64	• Sets the total number of stations (1 to 64) of I/O modules and remote terminal modules connected to A2C.	A2CCPU and A2CCPUC24(PRF)
D9036 D9037	For extension file register device number designation	Device number when accessing each device of an extension file register directly	• Designates the device number of an extension file register from/to which data is read/written to D9036 and D9037 as a BIN value. Designates the serial number from the R0 of block No.1 to the device number regardless of the block number. 	AnACPU-F
D9038 D9039	LED indication priority	Priority 1 to 4 Priority 5 to 7	• Sets priority of ERROR LEDs which illuminate (or flicker) to indicate errors with error code numbers. Configuration of the priority setting areas is as shown below. b15 ~ b12 b11 ~ b8 b7 ~ b4 b3 ~ b0 D9038: Priority 4 | Priority 3 | Priority 2 | Priority 1 D9039: | | Priority | • For details, refer to the A2CCPU User's Manual.	AnACPU-F, A2CCPU, A2CCPUC24(PRF) and A1SCPU
D9044	For sampling trace	Step or time for sampling trace	• To operate sampling trace [STRA] or [STRAR] by turning ON/OFF M9044 by peripheral devices, the value stored in D9044 is used as a condition for sampling trace. Scan : 0 Time : Time (per 10 msec) Value is stored in BIN code into D9044	All CPUs
D9050	SFC program error code	Code number of error occurred in the SFC program	• Stores code numbers of errors occurred in the SFC program in BIN code. 0 : No error 80 : SFC program parameter error 81 : SFC code error 82 : Number of steps of simultaneous execution exceeded 83 : Block start error 84 : SFC program operation error (For details, refer to section 7)	
D9051	Error block	Block number in which an error occurred	• Stores the block number in which an error occurred in the SFC program in BIN code. In the case of error 83, the starting block number is stored.	
D9052	Error step	Step number in which an error occurred	• Stores the step number in which error 83 occurred in the SFC program in BIN code. • Stores "0" when errors 80, 81, or 82 occurred. • Stores the block starting step number when error 83 occurred.	
D9053	Error transfer	Transition number in which an error occurred	• Stores the transition number in which error 84 occurred in the SFC program in BIN code. • Stores "0" when errors 80, 81, 82, or 83 occurred.	
D9054	Error sequence step	Sequence step number in which an error occurred	• Stores the sequence step number of transition and operation output in which error 84 occurred in the SFC program in BIN code.	
D9055	Status latch step number	Status latch step	• Stores the step number when status latch is executed.	AnACPU-F
D9061	Communication error code	0 : Normal 1 : Initial data error 2 : Line error	• Stores error code when M9061 is turned ON (communication with I/O modules or remote terminal modules fails). • 1 ..... Total number of stations of I/O modules or remote terminal modules or number of retries is not normal. Initial program contains an error. • 2 ..... Cable breakage or power supply of I/O modules or remote terminal modules is turned off.	A2CCPU and A2CCPUC24(PRF)
D9072	PC communication check	Data check by AJ71C24(S3)	• In the loopback test mode of individual AJ71C24(S3), the AJ71C24(S3) automatically executes data write/read and communication check.	All CPUs
D9081	Number of communication requests executed to remote terminal modules	0 to 32	• Stores the number of communication requests executed to remote terminal modules connected to AJ71PT32(S3) or A2CCPU. • Subtracts 1 at completion of communication with a remote terminal module.	AnACPU-F, A2CCPU and A2CCPUC24(PRF)
D9082	Final connected station number	Final connected station number	• Stores the final station number of I/O modules and remote terminal modules connected to A2C.	A2CCPU and A2CCPUC24(PRF)

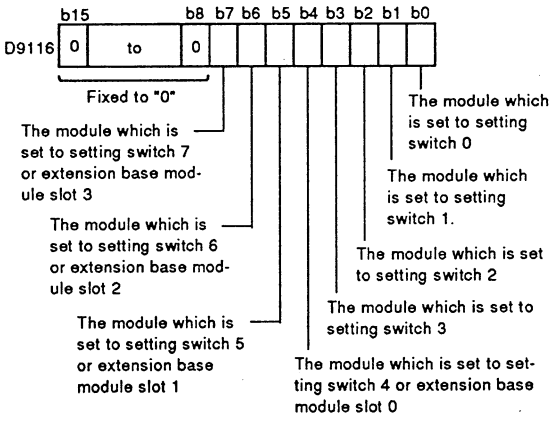
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>D9090</td><td>Micro-computer subroutine input data area head device number</td><td>Depends on the microcomputer program package to be used</td><td>• For details, refer to the manual of each microcomputer program package.</td><td rowspan="2">Except for AnACPU-F</td></tr>
<tr><td>D9091</td><td>Error code during a microcomputer subroutine call</td><td>Depends on each microcomputer package</td><td>• For details, refer to the manual of each microcomputer program package.</td></tr>
<tr><td>D9091</td><td>Instruction error</td><td>Instruction error detail number</td><td>• Stores an instruction error detail factor in code.</td><td>AnACPU-F</td></tr>
<tr><td>D9094</td><td>Changed I/O module head address</td><td>Changed I/O module head address</td><td>• Stores upper 2 digits of the head I/O address of I/O modules to be loaded or unloaded during online mode in BIN code.
Example: Input module X2F0 → H2F</td><td rowspan="9">AnNCPU-F and AnACPU-F</td></tr>
<tr><td>*2 D9100
*1 D9101
*1 D9102
*1 D9103
*1 D9104
*1 D9105
*1 D9106
*1 D9107</td><td>Fuse blow module</td><td>Bit pattern in units of 16 points of fuse blow modules</td><td>• Output module numbers (in units of 16 points), of which fuses have blown, are entered in bit pattern. (Preset output unit numbers when parameter setting has been performed)


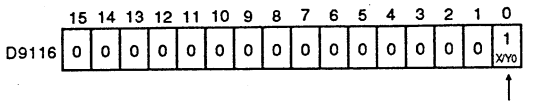
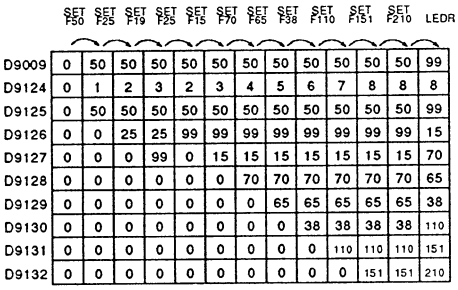
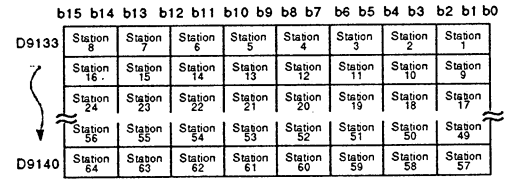
(If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)</td></tr>
<tr><td>*1 D9100</td><td>Fuse blown module</td><td>Bit pattern of fuse blown modules</td><td>• The output module number in the fuse blown state is entered in the bit pattern.

</td><td>A0J2HCPU</td></tr>
<tr><td>*1 D9100</td><td>Fuse blown module</td><td>The bit pattern in units of 16 points of fuse blown modules</td><td>• Output module numbers(in units of 16 points) whose fuses are blown or whose external power supply is off are entered in bit patterns. (When parameter setting has been performed, the set I/O module number is entered.)


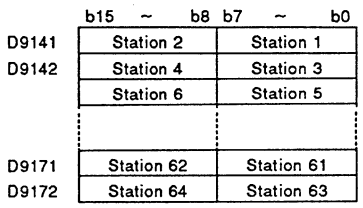
(When the normal status has been restored, this will not be cleard. Therefore, clearing must be done by the user's program.)</td><td>A1SCPU</td></tr>
</table>

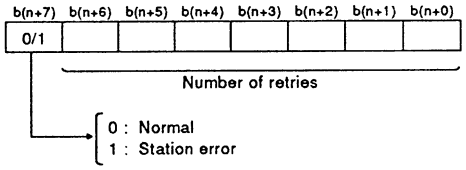
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>*2
D9108</td><td>Step transfer monitoring timer setting (for M9108)</td><td rowspan="7">Timer setting value and the F number at time out</td><td rowspan="7">• Sets value for the step transfer monitoring timer and the number of F which turns on when the monitoring timer timed out.
 

• By turning on any of M9108 to M9114, the monitoring timer starts. If the transition following a step which corresponds to the timer is not established within set time, the set annunciator (F) is turned on.</td><td rowspan="7">All CPUs</td></tr>
<tr><td>*2
D9109</td><td>Step transfer monitoring timer setting (for M9109)</td></tr>
<tr><td>*2
D9110</td><td>Step transfer monitoring timer setting (for M9110)</td></tr>
<tr><td>*2
D9111</td><td>Step transfer monitoring timer setting (for M9111)</td></tr>
<tr><td>*2
D9112</td><td>Step transfer monitoring timer setting (for M9112)</td></tr>
<tr><td>*2
D9113</td><td>Step transfer monitoring timer setting (for M9113)</td></tr>
<tr><td>*2
D9114</td><td>Step transfer monitoring timer setting (for M9114)</td></tr>
<tr><td>*1
D9116</td><td rowspan="8">I/O module verify error</td><td rowspan="8">Bit pattern in units of 16 points of verify error units</td><td rowspan="8">• When I/O modules, of which data are different from those entered at power-on, have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers when parameter setting has been performed)
 

(If normal status is restored, clear is not performed. Therefore, it is required to perform clear by use program.)</td><td rowspan="8">AnNCPU-F and AnACPU-F</td></tr>
<tr><td>*1
D9117</td></tr>
<tr><td>*1
D9118</td></tr>
<tr><td>*1
D9119</td></tr>
<tr><td>*1
D9120</td></tr>
<tr><td>*1
D9121</td></tr>
<tr><td>*1
D9122</td></tr>
<tr><td>*1
D9123</td></tr>
<tr><td>*1
D9116</td><td>I/O module verify error</td><td>Bit pattern of a verify error module</td><td>• When a different I/O module from the I/O module information registered when the power supply was turned ON is detected, the I/O module number is entered in the bit pattern.
 
</td><td>A0J2HCPU</td></tr>
</table>

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>*1
D9116</td><td>I/O module verify error</td><td>Bit pattern in units of 16 points of a verify error module</td><td>• When a different I/O module from the I/O module information registered when the power supply was turned ON is detected, the I/O module number(in units of 16 points) is entered.
(When parameter setting has been performed, the set I/O module number is entered.)
 
(When the normal status has been restored, this is not cleared. Therefore, clearing must be done by the user's program.)</td><td>A1SCPU</td></tr>
<tr><td>D9124</td><td>Annunciator detection quantity</td><td>Annunciator detection quantity</td><td>• When one of F0 to 255 is turned ON by [OUT F] or [SET F], 1 is added to the contents of D9124. When [RST F] or [LEDR] instruction is executed, 1 is subtracted from the contents of D9124. (If the INDICATOR RESET switch is provided to the CPU, pressing the switch can execute the same processing) Quantity, which has been turned ON by [OUT F] or [SET F] is stored into D9124 in BIN code. The value of D9124 is maximum 8.</td><td rowspan="2">All CPUs</td></tr>
<tr><td>D9125
D9126
D9127
D9128
D9129
D9130
D9131
D9132</td><td>Annunciator detection number</td><td>Annunciator detection number</td><td>• When one of F0 to 255 is turned ON by [OUT F] or [SET F], F number, which has turned ON, is entered into D9125 to D9132 in due order in BIN code. F number, which has been turned OFF by [RST F], is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the succeeding data registers. By executing [LEDR] instruction, the contents of D9125 to D9132 are shifted upward by one. (For A3N, it can be performed by use of INDICATOR RESET switch on front of CPU module) When there are 8 annunciator detections, the 9th one is not stored into D9125 to 9132 even if detected.
  </td></tr>
<tr><td>D9133
D9134
D9135
D9136
D9137
D9138
D9139
D9140</td><td>Remote terminal card information</td><td>00 : No I/O module or remote terminal module or initial communication impossible
01 : Input module or remote terminal module
10 : Output module</td><td>• Stores information of I/O modules and remote terminal modules connected to the A2C corresponding to station number.
Information of I/O modules and remote terminal modules is for input, output and remote terminal module identification and expressed as 2-bit data.
• 00 : No I/O module or remote terminal module or initial communication is impossible
• 01 : Input module or remote terminal module
• 10 : Output module
• Data configuration
  </td><td>A2CCPU and A2CCPUC24(PRF)</td></tr>
</table>

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>D9141
D9142
D9143
D9144
D9145
D9146
D9147
D9148
D9149
D9150
D9151
D9152
D9153
D9154
D9155
D9156
D9157
D9158
D9159
D9160
D9161
D9162
D9163
D9164
D9165
D9166
D9167
D9168
D9169
D9170
D9171
D9172</td><td>Number of times of retry execution</td><td>Number of retries</td><td>• Stores the number of retries executed to I/O modules or remote terminal modules which caused communication error. (Retry processing is executed the number of times set at D9174.)
• Data becomes 0 when communication is restored to normal.
• Station number setting of I/O modules and remote terminal modules is as shown below.
 

• Retry counter uses 8 bits for one station.
 

* "n" is determined by station number of I/O module or remote terminal module.
Odd number stations
(station 1, 3, 5, 7 ... 61, 63) : b0 to b7 (n = 0)
Even number stations
(station 2, 4, 6, 8 ... 62, 64) : b8 to b15 (n = 8)</td><td rowspan="4">A2CCPU and A2CCPUC24(PRF)</td></tr>
<tr><td>D9173</td><td>Mode setting</td><td>0 : Automatic online return enabled
1 : Automatic online return disabled
2 : Transmission stop at online error
3 : Line check</td><td>• Mode setting
0 | Automatic online return enabled | • When an I/O module or a remote terminal module caused communication error, the station is placed offline. Communication with normal stations is continued.
• When a faulty station returned to normal, communication is resumed automatically.
1 | Automatic online return disabled | • When an I/O module or a remote terminal module caused communication error, the station is placed offline. Communication with normal stations is continued.
• Though a faulty station returned to normal, communication is not restored unless the station module is restarted.
2 | Transmission stop at online error | • When an I/O module or a remote terminal module caused communication error, communication with all stations is stopped.
• Though a faulty station returned to normal, communication is not restored unless the station module is restarted.
3 | Line check | • Checks hardware and connecting cables of I/O modules and remote terminal modules.</td></tr>
<tr><td>D9174</td><td>Setting of the number of retries</td><td>Number of retries</td><td>• Sets the number of retries executed to I/O modules and remote terminal modules which caused communication error.
• Sets for 5 times at power on.
• Set range: 0 to 32
• If communication with an I/O module or a remote terminal module is not restored to normal after set number of retries, such module is regarded as a faulty station.</td></tr>
<tr><td>D9175</td><td>Line error retry counter</td><td>Number of retries</td><td>• Stores the number of retries executed at line error (time out).
• Data becomes 0 when line is restored to normal and communication with I/O modules and remote terminal modules is resumed.</td></tr>
</table>

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th>Applicable CPU</th></tr>
<tr><td>D9180
D9181
D9182
D9183
D9184
D9185
D9186
D9187
D9188
D9189
D9190
D9191
D9192
D9193</td><td>Remote terminal module error number</td><td></td><td>• Stores error code of a faulty remote terminal module when M9060 is turned on.
• The error code storage areas for each remote terminal module are as shown below.

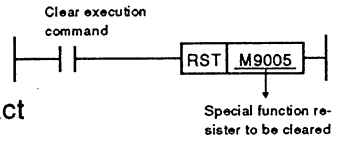
D9180 Remote terminal module No. 1
D9181 Remote terminal module No. 2
D9182 Remote terminal module No. 3
⋮
D9192 Remote terminal module No. 13
D9193 Remote terminal module No. 14
Remote terminal module numbers from 1 to 14 are set with D9020 to D9034.</td><td rowspan="5">A2CCPU and A2CCPUC24(PRF)</td></tr>
<tr><td>D9196</td><td rowspan="4">Faulty station detection</td><td rowspan="4"></td><td>• Error code is cleared in the following cases.
• When the RUN key switch is moved from STOP to RUN. (D9180 to D9183 are all cleared)
• When Yn4 of each remote terminal is set from OFF to ON.</td></tr>
<tr><td>D9197</td><td>• Bit which corresponds to faulty I/O module or remote terminal module is set (1).
[Bit which corresponds to a faulty station is set when normal communication cannot be restored after executing the number of retries set at D9174.]
• If automatic online return is enabled, bit which corresponds to a faulty station is reset (0) when the station is restored to normal.
• Data configuration</td></tr>
<tr><td>D9198</td><td rowspan="2">Address b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
D9196 Station 16 Station 15 Station 14 Station 13 Station 12 Station 11 Station 10 Station 9 Station 8 Station 7 Station 6 Station 5 Station 4 Station 3 Station 2 Station 1
D9197 Station 32 Station 31 Station 30 Station 29 Station 28 Station 27 Station 26 Station 25 Station 24 Station 23 Station 22 Station 21 Station 20 Station 19 Station 18 Station 17
D9198 Station 48 Station 47 Station 46 Station 45 Station 44 Station 43 Station 42 Station 41 Station 40 Station 39 Station 38 Station 37 Station 36 Station 35 Station 34 Station 33
D9199 Station 64 Station 63 Station 62 Station 61 Station 60 Station 59 Station 58 Station 57 Station 56 Station 55 Station 54 Station 53 Station 52 Station 51 Station 50 Station 49
1 : Error
0 : Normal</td></tr>
<tr><td>D9199</td></tr>
</table>

POINTS

(1) Special registers are cleared when the PC is switched OFF or the RESET switch is set to LATCH CLEAR or RESET. Data remains unchanged when the RUN key switch is set to STOP.

(2) Special registers marked *1 above are latched and their data will remain unchanged after normal status is restored. Therefore, use the method as shown below to clear the data.

1) Method by user program
Insert the circuit shown at right into the program and turn ON the clear execution command contact to clear the contents of register.



2) Method by peripheral device
Set the register to "0" by changing the present value by the test function of peripheral device or set to "0" by forced reset. For the operation procedure, refer to the Instruction Manual for peripheral device.

3) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

(3) Data is written to special registers marked *2 above in the sequence program.

(4) Data is written to special registers marked *3 above in test mode of the peripheral device.

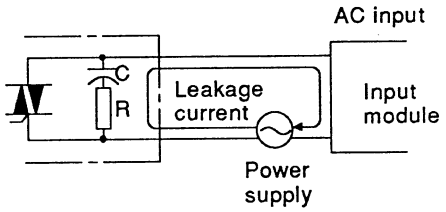
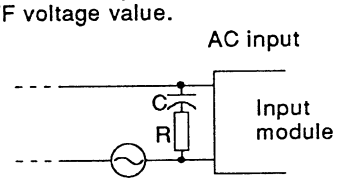
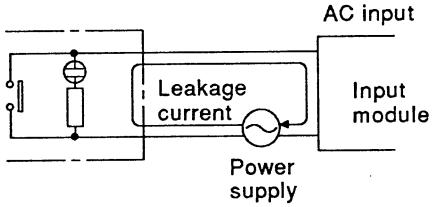
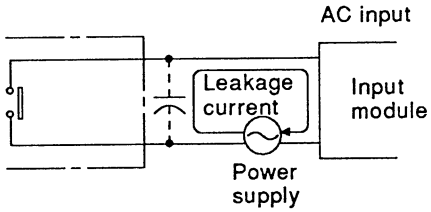
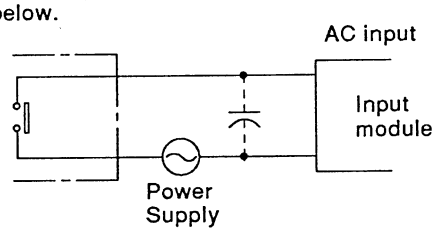
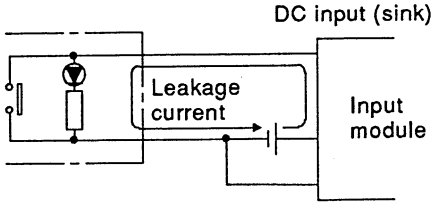
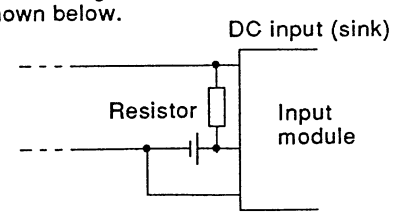
1.4 I/O Connection Troubleshooting

This section explains possible problems with I/O circuits.

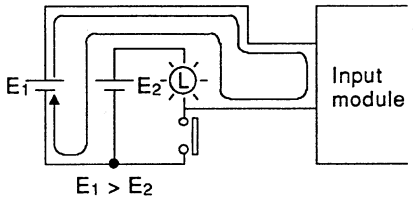
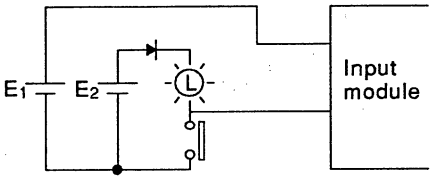
1.4.1 Input circuit troubleshooting

This section describes possible problems with input circuits, and corrective actions.

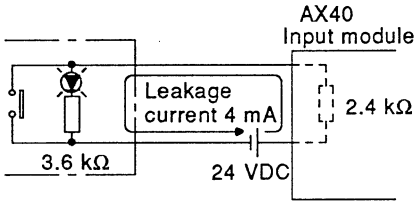
Input Circuit Problems and Corrective Actions

	Condition	Cause	Corrective Action
Example 1	Input signal does not turn OFF.	• Leakage current of input switch (such as drive by non-contact switch). 	• Connect an appropriate register which will make the voltage across the terminals of the input module lower than the OFF voltage value.  It is recommended to use 0.1 to 0.47 μF + 47 to 120 Ω (1/2 W) for the constant of CR.
Example 2	Input signal does not turn OFF.	• Drive by a limit switch with neon lamp. 	• Same as Example 1. • Or make up another independent display circuit.
Example 3	Input signal does not turn OFF.	• Leakage current due to line capacity of wiring cable. Line capacity C of twisted pair wire is approx. 100 PF/m(39.37 inches). 	• Same as Example 1. • However, leakage current is not generated when power supply is located on the input equipment side as shown below. 
Example 4	Input signal does not turn OFF.	• Drive by switch with LED indicator. 	• Connect a register which will make the voltage across input module terminal and common higher than the OFF voltage, as shown below.  * The calculation example of connected resistor value is shown in the following page.

Input Circuit Problems and Corrective Actions (Continue)

	Condition	Cause	Corrective Action
Example 5	Input signal does not turn OFF.	• Sneak path due to the use of two power supplies. 	• Use only one power supply. • Connect a sneak path prevention diode. (Figure below) 

Calculation example for Example 4

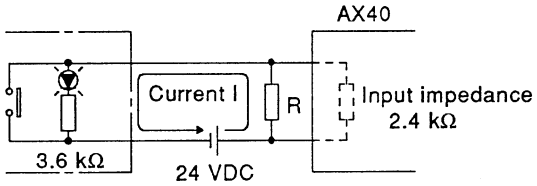


The switch with the LED indicator is connected to AX40 and there is a 4 mA leakage current.

- The voltage VTB across terminal and common is obtained using the following formula:

V_{TB} = 4 [mA] x 2.4 [kΩ] = 9.6 [V] (The voltage drop of the LED is ignored.)

Since this voltage does not satisfy the OFF voltage of 6 [V] or lower, the input signal does not turn off. Therefore, connect a resistor as shown below.



- Calculate the resistor value R, as shown below:
  For an input voltage < 6 V, current 1 must be:

(24 – 6 [V]) ÷ 3.6 [kΩ] = 5 mA

Resistor R must be selected to give a current of 1 > 5 mA.

- Hence, for resistor, R

  6 [V] ÷ R > 5 [mA] – 6 [V]/2.4 [kΩ]
  6 [V] ÷ 2.5 [mA] > R
  2.4 [kΩ] > R

  For R = 2 [kΩ], the power capacity must be:

  W = (applied voltage)^2 /R (or W = (maximum current)^2 x R)

  Resistor R terminal voltage is:

  $$\frac{2.4 \times 2}{2.4 + 2}\ [K\Omega] : \frac{2.4 \times 2}{2.4 + 2} + 3.6\ [K\Omega] = X : 24\ [V]$$

  X = 5.58 [V]

  Therefore, the power capacity W of resistor R is

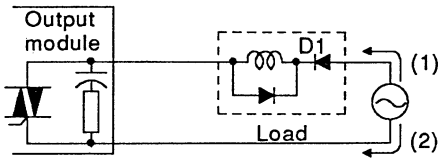
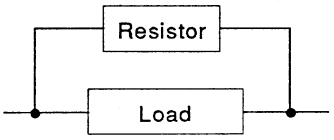
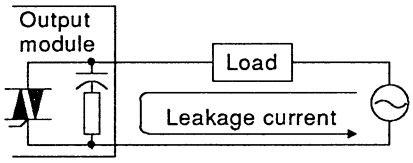
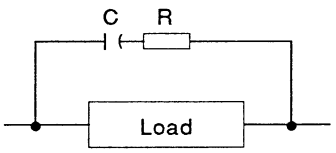
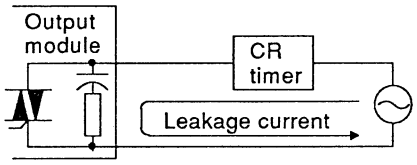
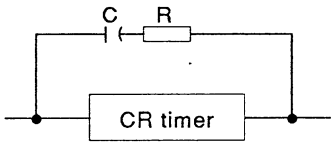
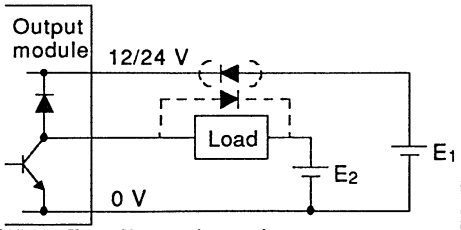
  W = (5.58 [V])^2 /2 [kΩ] = 0.015 [W]

- Use a safety factor of 3 to 5. The resistor should therefore be rated at 0.5 to 1 W.

  A 3 kΩ, 0.5 to 1 W resistor should therefore be connected across the relevant input terminal and its COM.

1.4.2 Output circuit failures and corrective actions

Output Circuit Failures and Corrective Actions

	Condition	Cause	Corrective Action
Example 1	When the output is OFF, excessive voltage is applied to the load.	• Load is half-wave rectified inside (Seen in some solenoids). AY22,AY23  • When the polarity of the power supply is as shown in [1], C is charged. When the polarity is as shown in [2], the voltage charged in C plus the line voltage are applied across D1. Max. voltage is approx. 2.8E.	• Connect a resistor of several 10 kΩ to several hundred kΩ across the load. If a resistor is used in this way, it does not pose a problem to the output element. But it may cause the diode, which is built in the load, to deteriorate, resulting in a fire, etc. 
Example 2	The load does not turn OFF (triac output).	• Leakage current due to built-in noise suppression AY22, AY23 	• Connect C and R across the load. When the wiring distance from the output card to the load is long, there may be a leakage current due to the line capacity. 
Example 3	When the load is a C-R type timer, time constant fluctuates (triac output).	AY22, AY23 	• After driving the relay, drive the C-R type timer by the same contact. Some timers have half-wave rectified internal circuits. Therefore, take the precautions indicated in the example. 
Example 4	Load does not turn OFF. (For direct current)	• Sneak path due to the use of two power supplies. AY40, 41, 42  • When $E_1 < E_2$, snake path occurs.	• Reduce the power supplies form two to one. • Connect a sneak path prevention diode. When the load is a relay or similar device, it is necessary to connect reverse-voltage absorbing diode to the load. (Shown by the dotted line in the figure at left)

2. COMMON ITEMS OF SPECIAL-FUNCTION MODULES

Details about analog-to-digital conversion modules and digital-to-analog conversion modules are given in Section 3. Section 4 gives details about high-speed counter module troubleshooting.
In addition, there are many other different kinds of special-function modules. This section explains the common items that should be known to do troubleshooting of special-function modules.

2.1 Special-Function Modules

Special-function modules are designed to execute functions which cannot be done by a PC CPU or functions whose applications are limited.
The principal special-function modules are as follows:

(1) Analog-to-digital conversion

An analog (±10 V, 4 to 20 mA) is input.

(2) Digital-to-analog conversion

An analog (±10 V, 4 to 20 mA) is output.

(3) High-speed counter

High-speed pulses, encoders, etc. are input.

(4) Positioning

High-speed pulses are output to a positioning servo amplifier.

(5) Graphic controllers

Graphics are monitored on CRT, LCD, and plasma display screens.

(6) RS-232C, RS-422, and parallel interfaces

Data links are executed by connecting other computers, a printers, bar code readers, ID plates, etc.

(7) Audio output

Audio recorded by using a microphone is announced from the speaker when necessary.

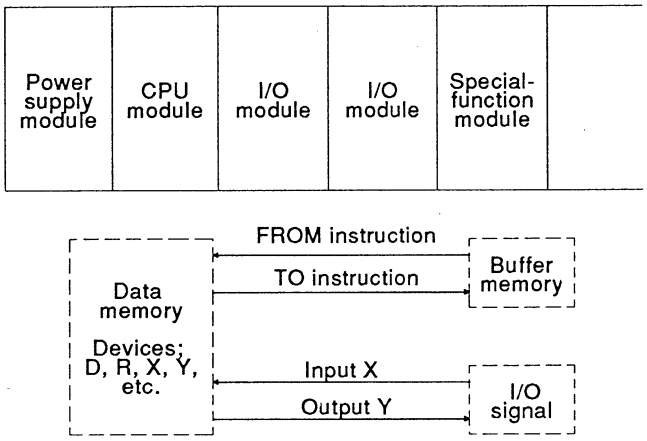
(8) External fault diagnosis

Diagnoses whether or not input signals and external output signals are operating correctly. If there is a malfunction, it is detected.

2.2 Relationship Between PC CPUs and Special-Function Modules

Special-function modules have a buffer memory and can store necessary data to the buffer memory.
A PC CPU can write data to a buffer memory by using a TO instruction and can read data from the buffer memory by using a FROM instruction from the buffer memory as necessary.

When a command is sent from a PC CPU to a special-function module, output signal Y goes ON and OFF. When a special-function module returns a response to the PC CPU, input signal X goes ON and OFF.



The User's Manual of the applicable special-function module give details about I/O signal and buffer memory allocations.

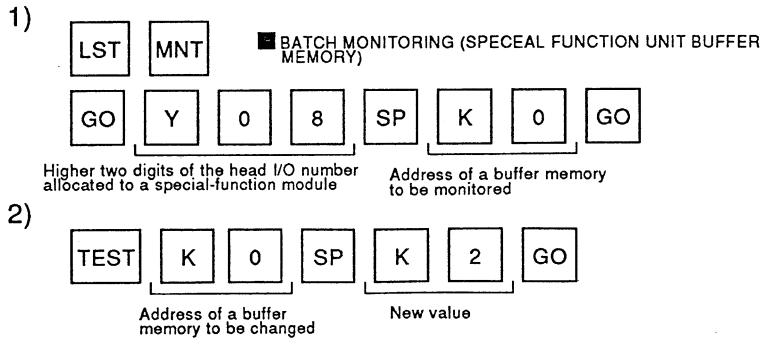
---------Signal example----------

When a special-function module malfunctions, the WDT error signal (X00) goes ON.
Thus, errors can be read by using PC CPU programs.

2.3 Buffer Monitoring and Forcible Changing of Current Values by Using Peripheral Devices

Current values can be checked by directly monitoring a buffer memory using an A6GPP or A6PHP (SW4GP-GPPA).

(1) Monitoring operation/current value change operation by A6GPP



I/O No. 08	*BATCH MONITORING (SPECIAL FUNCTION UNIT BUFFER MEMORY)*				
ADDRESS		ADDRESS		ADDRESS	
0	2	16	7	32	5
1	0	17	5	33	0
2	0	18	1	34	1
3	0	19	0	35	0
4	0	20	500	36	0
5	0	21	0	37	0
6	0	22	7	38	0
7	0	23	0	39	0
8	0	24	8	40	0
9	0	25	0	41	0
10	1	26	7	42	0
11	500	27	0	43	0
12	7	28	8	44	0
13	8	29	0	45	0
14	7	30	7	46	0
15	8	31	0	47	0

3. A-D, D-A CONVERSION MODULES

This section explains the error descriptions and troubleshooting which can occur when analog-to-digital and digital-to-analog modules are used.

3.1 A0J2-68AD, A68AD Analog-to-Digital Conversion Module

3.1.1 Write date error code list

The following three errors may occur during the write operation of the number of channels, averaging processing specification, averaging time, and averagin count. The numeric value of the error code enclosed in [ ] indecates the channel number for which the error has occurred.

Types of Write Data Error Codes

Description	Error Code*1
A value other than 0 to 8 has been set as the number of channels.	01
A value other than 20 to 10000 ms has been set as an averaging time set value.	[ ] 0 to 4
A value other than 1 to 4000 times has been set as an averaging count set value.	[ ] 5 to 8

POINTS

(1) [ ] 0 to 4 and [ ] 5 to 8 of write data error code are used only to make differentiation between averaging time and averaging count, respectively. The individual numerals do not have any significance.

(2) When an error has occurred, check the write data error code*2, reset the error code, and then write the corrected data. (Refer to Section 3.4.2 on page 3-13.)

Example:

(1) Error code 32 has occurred

Since the averaging time of channel 3 is wrong, change the value to within the range 20 to 10000ms.

(2) Error code 88 has occurred

Since the averaging count of channel 8 is wrong, change the value to within the range 1 to 4000 times.

(Note)

*1 Error codes are stored in binary in buffer memory address 34.

a) When data is written from a PC CPU, the analog-to-digital conversion module checks the data ranges of the number of used channels, the average number of times, and 1 time only averages.
when data is outside a range, error codes are 16 bit binary.

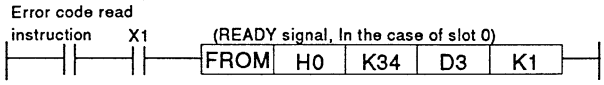
b) Error codes can be reset by writing 0 from the PC CPU.

c) When several error codes occur, the writing data error which was found first by an analog-to-digital conversion module is stored.
Subsequent errors are not stored.

d) If an error is reset without correcting that error, the writing data error code becomes 0, and RUN LED of an analog-to-digital conversion module stops flickering and goes ON.

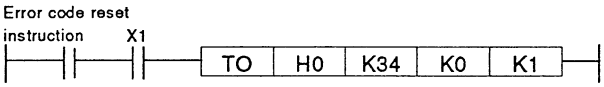
*2 The error code is read by using a FROM instruction.
Error reset is executed with the program from the PC CPU by using a TO instruction.

a) When an error code is read to D3



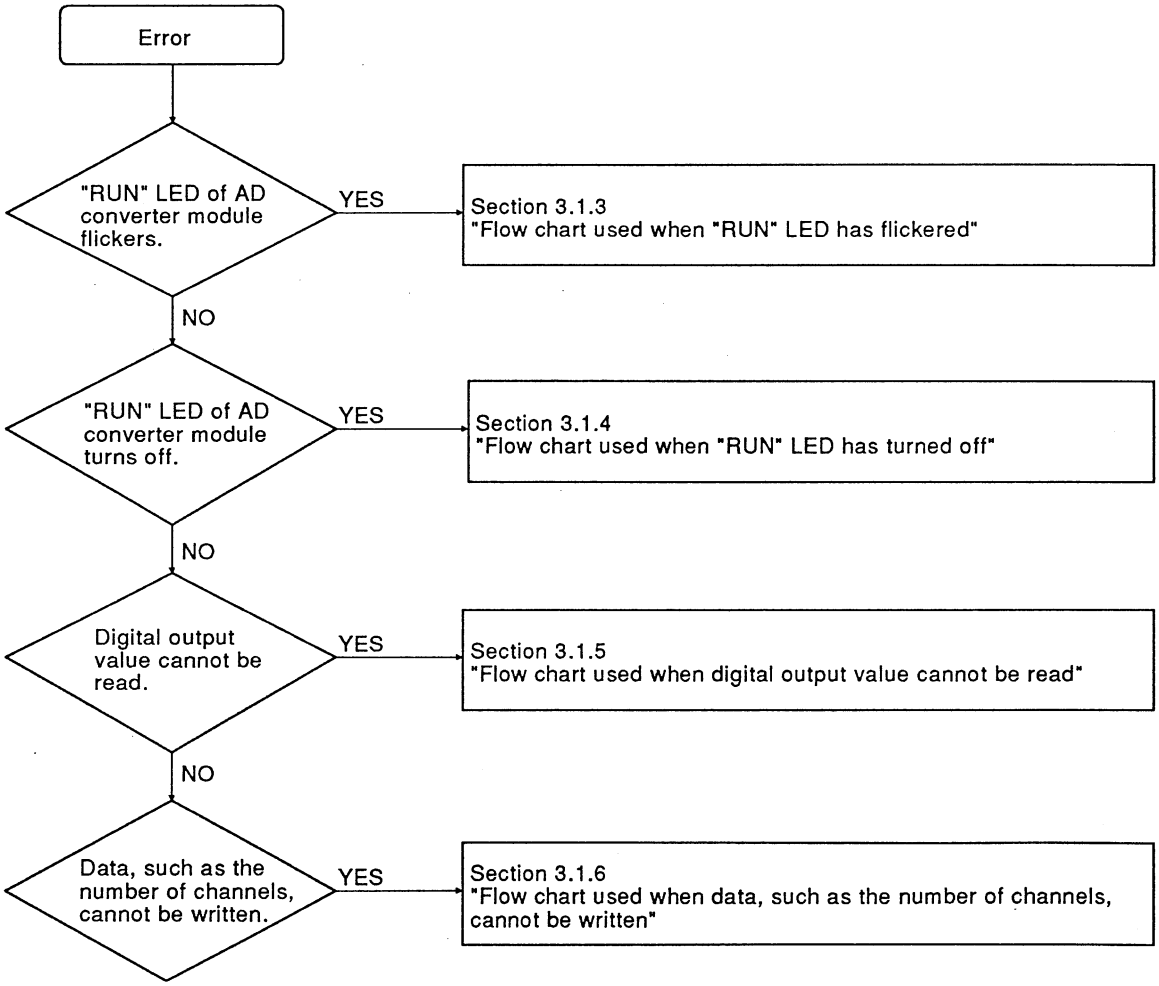
An error code is read to D3.

b) When an error code is reset

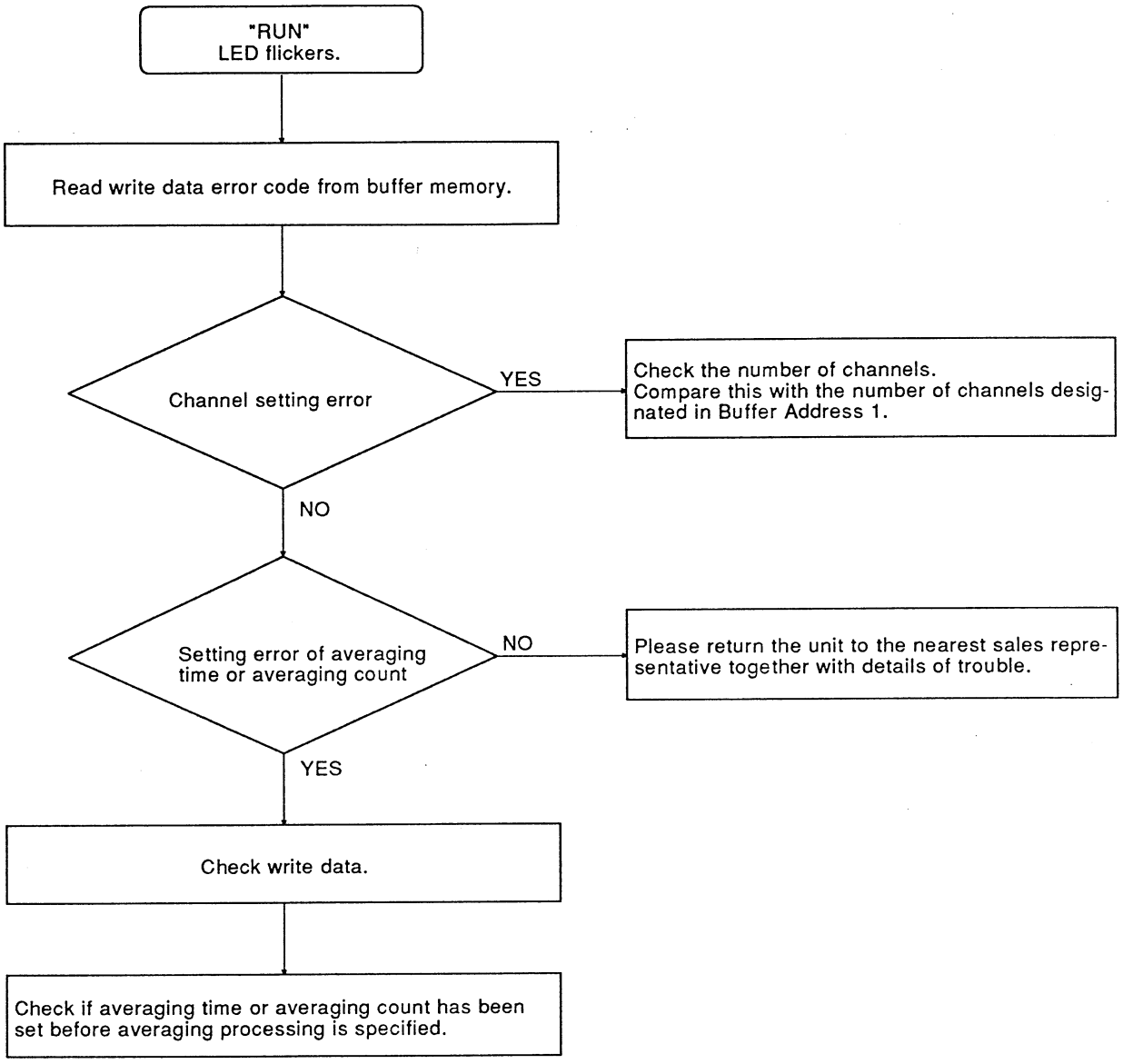


0 is written to buffer memory address 34, and the error code is reset.

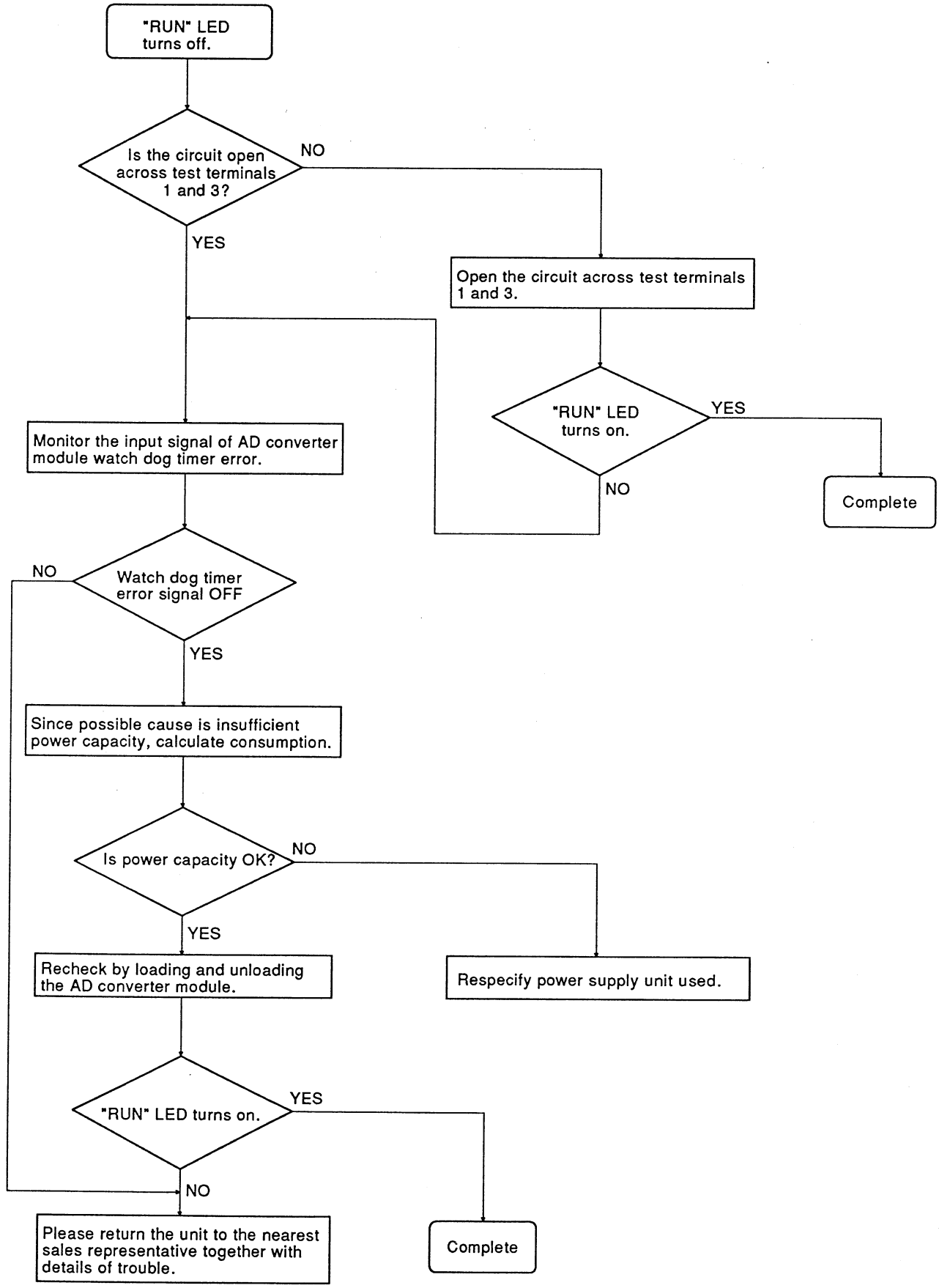
3.1.2 Troubleshooting flow chart



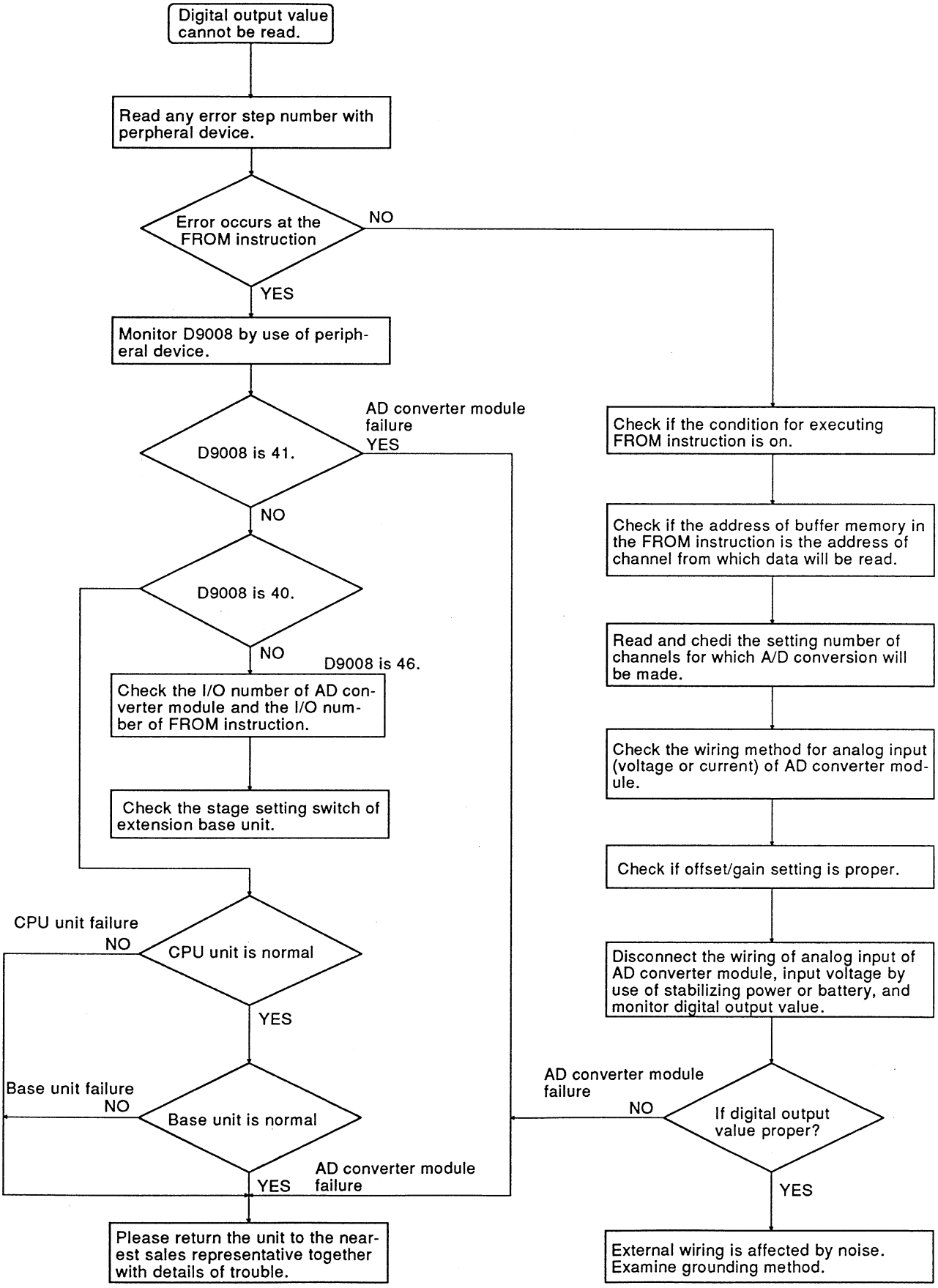
3.1.3 Flow chart used when "RUN" LED has flickered



3.1.4 Flow chart used when "RUN" LED has turned off



3.1.5 Flow chart used when digital output value cannot be read

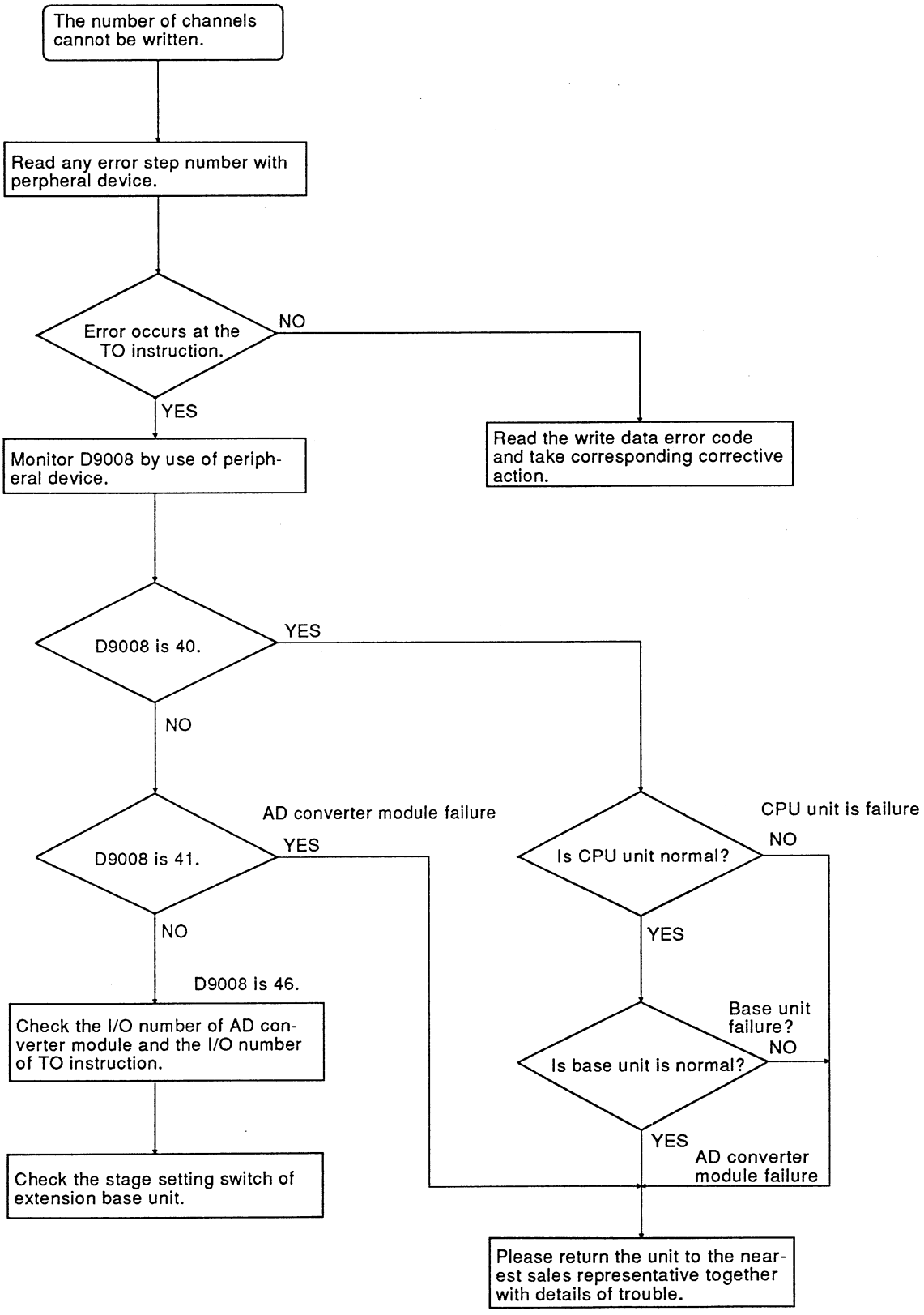


REMARK

The following contents are written into D9008 when an error has occurred during execution of the FROM or TO instruction to the AD converter module.

Content (BIN value) of Special Register D9008	CPU Status	Error and Cause
40	Stop	FROM and TO instructions cannot be executed. Hardware failure of AD converter module (special function unit), CPU unit, or base unit.
41	Stop	When the FROM or TO instruction has been executed, access has been made to the special function unit but no answer is returned. The accessed AD converter module (special function unit) has failed.
46	Stop (Continuous operation can be performed by the setting of parameter.)	Access has been made (FROM or TO instruction has been executed) to a slot where the AD converter module (special function unit) is not loaded. The content of FROM or TO instruction is incorrect or the stage number setting of extension base unit is incorrect.

3.1.6 Flow chart used when data, such as the number of channels, cannot be written



3.2 A68ADC Analog-to-Digital Conversion Unit

3.2.1 Error code list

If an error has occurred when data is written to the A68ADC (the RUN LED flickers), any of the error codes mentioned in the list below is stored in buffer memory at address 18.
When the A2CCPU is usesd, the same error code is stored also in special registers D9180 to D9193. When the AJ71PT32-S3 is used, the same error code is stored also in buffer memory at addresses 196 to 209.

Error Code	Cause	Corrective Action
100 (64_H)	(Read error) • Designated head address is out of buffer memory. • Designated range of read words includes addresses out of buffer memory.	Correct data which designates range out of buffer memory.
101 (65_H)	(Write error) • Designated head address is out of buffer memory. • Designated range of write words includes addresses out of buffer memory. • Write was attempted to read-only areas.	• Correct data which designates range out of buffer memory. • Correct data which designates range read-only areas.
102 (66_H)	Command code other than read (1) or write (2) is received.	Correct command code.
103 (67_H)	Data was received immediately after read command (1).	Correct the read execution instruction to disable data transmission.
104 (68_H)	Read and write word length is set at "0".	Set word length at "1" or over.
105 (69_H)	The number of words set by write command data differs from that of received data.	Match the number of words of command data with that of the data.
1 [ ] 0 to 4	Averaging time is set out of 20 to 10000 msec range. • [ ] indicates the channel in which the error occurred. • Numbers 0 to 4 do not have meaning, but indicate an averaging time error.	Correct averaging time setting in 20 to 10000 msec range.
1 [ ] 5 to 9	Averaging count is set out of 1 to 4000 counts. • [ ] indicates the channel in which the error occurred. • Numbers 5 to 9 do not have meaning, but indicate an averaging count error.	Correct averaging count setting in 1 to 4000 counts range.

(a) If two or more errors occur continuously, the error code for the first error is stored, and following error codes are not stored.

(b) Error code reset is done by writing "0" to address 18 of buffer memory. (Figures other than 0 are ignored.)

When the AJ71PT32-S3 is used, error codes for the errors occur during communication with remore terminal modules are stored in buffer memory at addresses 196 to 209 in addition to the error codes for errors detected by the A68ADC.

Error Code	Error Name	Cause	Corrective Action
1	Set data error	Data written to the remote terminal transmission areas includes errors.	Correct the data.
6	WDT error	Remote terminal module malfunction.	• Reset faulty remote terminal module. • Turn OFF and then ON the power. • If the above procedures do not recover the system, the system hardware is faulty. Please consult Mitsubishi representative.
8	Transmission area setting error	Remote terminal transmission area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.
9	Communication error	Communication between the master module and remote terminal modules is faulty.	Noise or remote terminal module failure.
10 (A_H)			
10 (A_H)	Receive area setting error	Remote terminal receive area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.

3.2.2 When the RUN LED flickers or turned OFF

(1) When flickers:

Check Point	Corrective Action
Data which disables write or read is written to the A64DAVC/DAIC.	Refer to the List of Error Codes (Section 3.2.1) for the cause, and correct the sequence program.

(2) When turned OFF:

Check Point	Corrective Action
24 VDC power supply is turned on.	Make sure the power supply.
24 VDC power supply voltage is within the set range.	Adjust the voltage within 15.6 to 31.2 V range.
If the MINI-S3 link is connected, the MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Add a loop to turn ON the MINI-S3 link communication start signal $Y_{(n+28)}$ to the sequence program.
If the MINI-S3 link is connected, error code "6" may be stored in the master module buffer memory at address 196 to 209.	Reset the PC CPU, and start them in the same manner. If error code "6" is again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
If the MINI-S3 link is connected, error codes "9" and "10" may be stored in the master module buffer memory at address 196 to 209.	Reset the PC CPU, and start them in the same manner. If error codes "9" and "10" are again stored, the system hardware may be fault. Please consult Mitsubishi representative.
Data link cables are normal.	Check the cables.
The TEST terminals are open.	After offset/gain setting, open the TEST terminals.

3.2.3 When the LINK RUN LED turned OFF or the LINK ERR. LED turned ON

Check Point	Corrective Action
The RUN LED is flickering.	Follow Section 3.2.2 (1).
The RUN LED turned OFF.	Follow Section 3.2.2 (2).

3.2.4 When read of digital output values is impossible

Check Point		Corrective Action
The RUN LED is flickering or turned OFF.		Follow Section 3.2.2.
The ERROR LED of the CPU module is flickering or turned ON.		Refer to the User's Manual for respective CPU module for error content.
The RUN LED of the CPU module is flickering or turned OFF.		Refer to the User's Manual for respective CPU module for error content.
When A2CCPU is used:	The RD/SD LED of the CPU unit is flickering. (normal)	Refer to the A2CCPU User's Manual for error content.
When AJ71PT32-S3 is used:	The MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Set the sequence program to turn ON the MINI-S3 link communication start signal.
	The RUN LED of the master module is turned OFF.	Refer to the AJ71PT32-S3 User's Manual for error content.
	The RD/SD LED of the master module is flickering. (normal)	Refer to the AJ71PT32-S3 User's Manual for error content.
Analog input signal lines are broken or disconnected.		Locate trouble by checking the signal lines visually and for continuity.

3.3 A1S64AD Analog-to-Digital Conversion Module

Assorted problem conditions and a troubleshooting guide for the A1S64AD are described below.

3.3.1 Error code list

When data is written to an A1S64AD from a PC CPU or an error occurs by reading data (RUN LED of A1S64AD flashes), the following error codes are stored in address 18 of the A1S64AD buffer memory.

Error Code List (Detected with A1S64AD)

Error Code	Cause	Corrective Action
100	Wrong number (other than 1 to 3) was set to the resolution.	Set the resolution to either 1, 2, or 3.
102	Data was written to the read-only area (addresses 10 to 13).	Modify the specified place for the read-only area.
[ ] 0	• A value outside 80 to 10000 msec was set for the average time. • [ ] indicates the channel No. in which an error occurred.	Set the average time within 80 to 10000 msec.
[ ] 5	• A value outside 1 to 500 times was set for the average count. • [ ] indicates the channel No. in which an error occurred.	Set the average count within 1 to 500 times.

(1) When several errors occur, the error code that occurred first is stored, and any errors after that are not stored.

(2) The error code is reset by turning ON Y12 with a sequence program.

3.3.2 Troubleshooting

The following explains the simple troubleshooting for A1S64AD. Refer to the CPU Module User's Manual for a PC CPU module.

(1) When the RUN LED of A1S64AD flashes

Items to Check	Corrective Actions
Is the data which cannot be executed read/write written to A1S64AD?	Confirm the error cause with the error code list in Section 3.3.1, and correct the sequence program.

(2) When the RUN LED of A1S64AD goes OFF

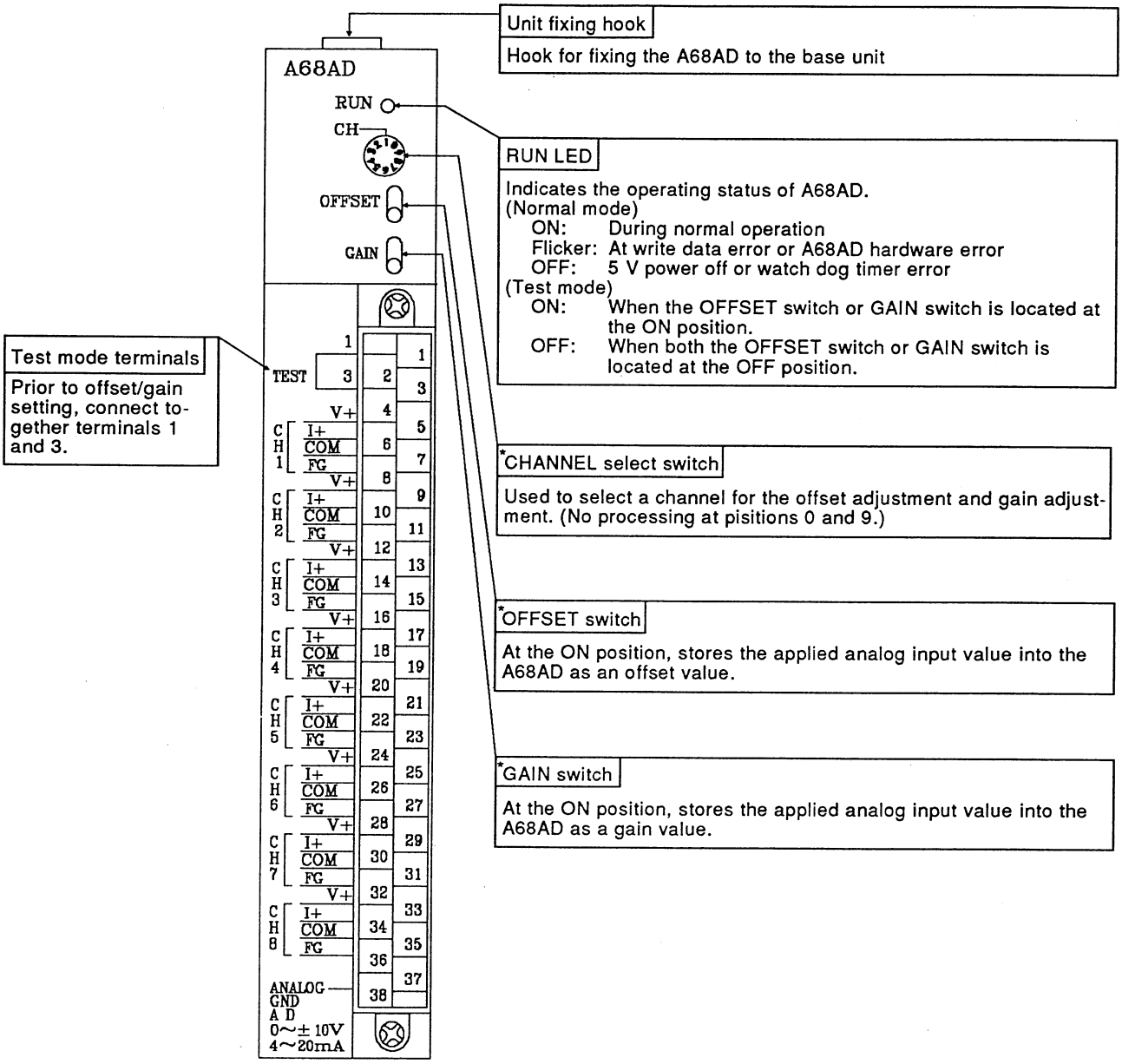
Items to Check	Corrective Actions
Are the TEST terminals opened?	Make offset/gain adjustments, and open the TEST terminals.
Is X0 (WDT error) set?	Reset the PC CPU. If the RUN LED is not turned ON after resetting a PC CPU, there may be a hardware malfunction in the module.

(3) When the digital output value cannot be read

Items to Check	Corrective Actions
Is the RUN LED of A1S64AD flashing or turned OFF?	Follow the procedures in above (1) or (2).
Is the ERROR LED of the CPU is turned ON?	Check the error description according to the CPU User's Manual.
Is the RUN LED of the CPU flashing or turned OFF?	Check the error description listed in the CPU User's Manual.
Is the condition to execute FROM instruction turned ON?	Monitor with a peripheral device such as GPP, and confirm whether it is ON or OFF.
Does the address of the buffer memory specified with a FROM instruction correspond to the address of the digital output value of channel to be read?	Check the sequence program.
Is the channel specified with FROM instruction set to A-D conversion enable?	Read the buffer memory address 0 and verify whether it is set to conversion enable or disable.
Is the conversion completed in the channel specified with FROM instruction?	Read the buffer memory address 19 and verify the conversion completed flag.
Is the analog input signal line disconnected, or does an error occur?	Confirm the error by visually checking or conduction checking the signal line.
Disconnect the analog input wire of A1S64AD, and apply the test voltage to the terminal of this module to measure the digital output value.	If the digital output value is normal with an A1S64AD, the module is affected by noise with external wiring. Therefore, check the wiring and grounding method.

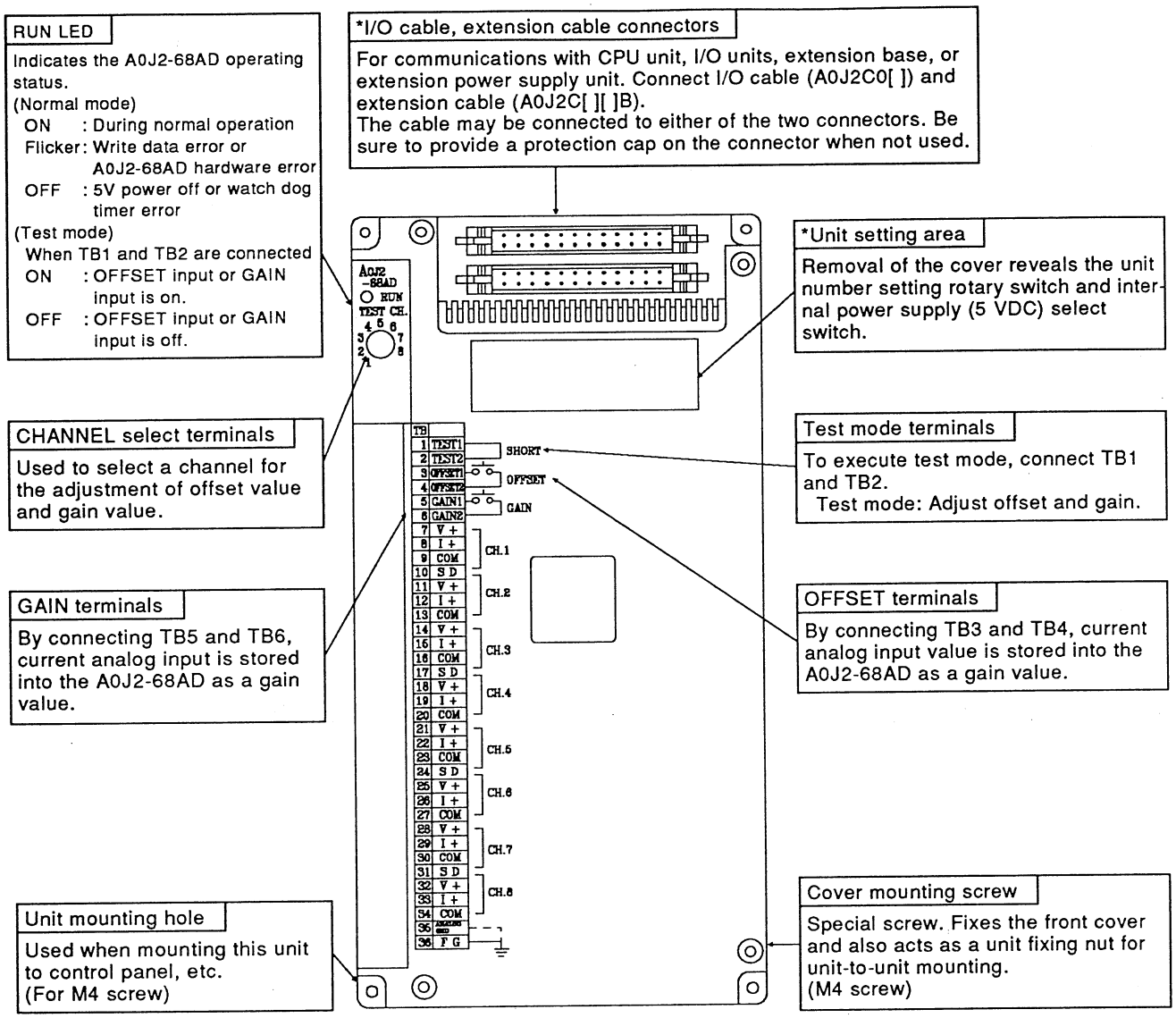
3.4 Nomenclature

3.4.1 A68AD



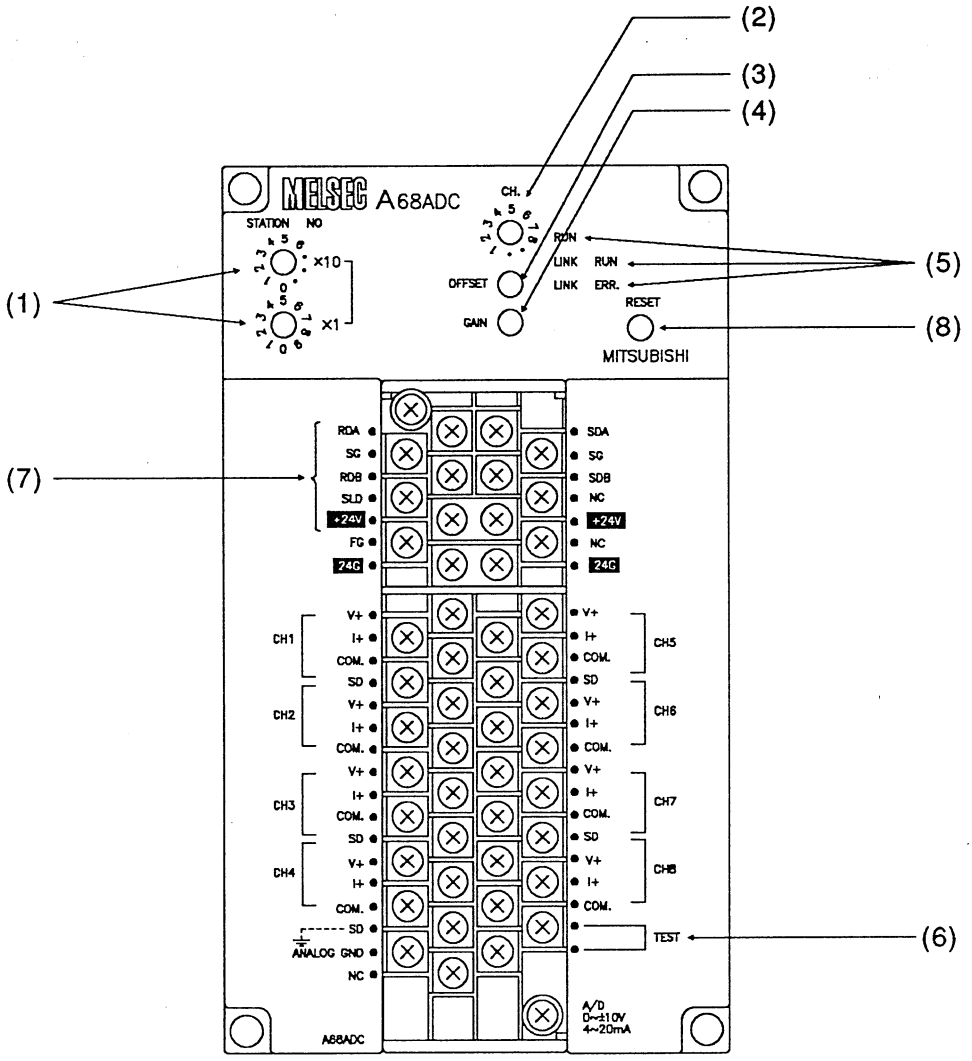
Switches marked * are valid only in test mode.

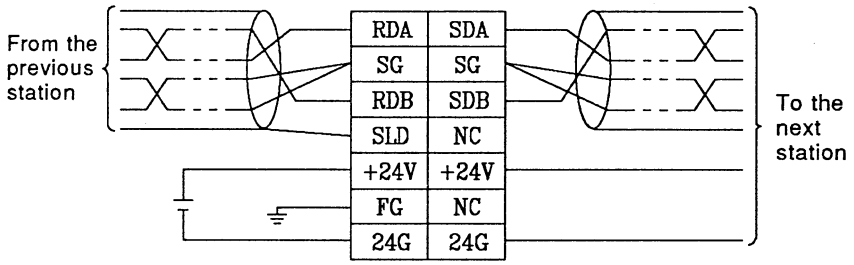
3.4.2 A0J2-68AD



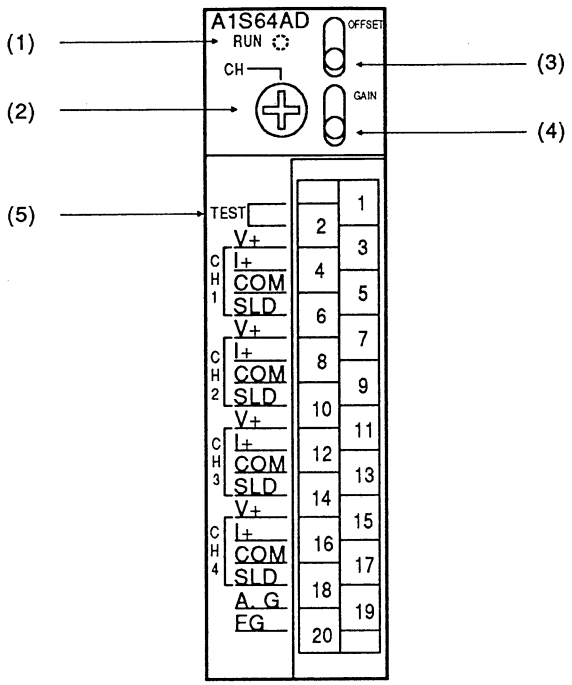
It is necessary to set the areas marked * prior to test operation and adjustments.

3.4.3 A68ADC


(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
MELSEC A68ADC
STATION NO
×10
×1
CH.
OFFSET
GAIN
RUN
LINK RUN
LINK ERR.
RESET
MITSUBISHI
RDA
SG
RDB
SLD
+24V
FG
24G
SDA
SG
SDB
NC
+24V
NC
24G
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
V+
I+
COM.
SD
ANALOG GND
NC
TEST
A68ADC
A/D
0~±10V
4~20mA

<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>(1)</td><td>Station number setting switches</td><td>(↓) x 10 (↓) x 1 Used to set the station number of the A68ADC in a range from 1 to (64 - occupied stations + 1).</td></tr>
<tr><td>(2)</td><td>Channel select switch</td><td>Used to select the channel for offset/gain adjustment.
(Positions 0 and 9 select no processing.)</td></tr>
<tr><td>(3)</td><td>OFFSET switch</td><td>By turning this ON in the TEST mode (short the TEST mode terminals), the analog input value at that time is stored as the offset value in the A68ADC.</td></tr>
<tr><td>(4)</td><td>GAIN switch</td><td>By turning this ON in the TEST mode (short the TEST mode terminals), the analog input value at that time is stored as the gain value in the A68ADC.</td></tr>
<tr><td>(5)</td><td>Operation state indicator LEDs</td><td>
<table>
<tr><td rowspan="2">RUN LED</td><td>Normal mode</td><td>On: Normally running
Flicker: Write data error
Off: 24 VDC is off or WDT error.</td></tr>
<tr><td>Test mode</td><td>On: OFFSET or GAIN switch is ON.
Off: OFFSET or GAIN switch is OFF.</td></tr>
<tr><td>LINK RUN LED</td><td>On:
Off:</td><td>Normal communication
Receive data error</td></tr>
<tr><td>LINK ERR LED</td><td>On:
Off:</td><td>Receive data error
Normal communication</td></tr>
</table>
</td></tr>
<tr><td>(6)</td><td>Test mode terminals</td><td>Shorted when setting offset/gain.</td></tr>
<tr><td>(7)</td><td>Terminal block for twisted pair cables and power supply cables</td><td> 
</td></tr>
<tr><td>(8)</td><td>Rest switch</td><td>Hardware reset
Used to initialize buffer memory and operation processing of the A68ADC.
By turning this ON, the control input signal X5 of the A68ADC turns ON.
(Device number of control I/O signals depends on station setting.)</td></tr>
</table>

3.4.4 A1S64AD



No.	Description	Application
(1)	"RUN" LED RUN	Indicates the operating status of the A1S64AD. (Normal mode) On : Indicates that the A1S64AD is operating without fault. Flash : Writing data error occurred. Off : External power 5 VDC is not supplied to the A1S64AD or A1S64AD is in WDT error (Test mode) On : OFFSET or GAIN switch is ON. Off : OFFSET and GAIN switches are OFF.
(2)	Channel select switch CH	Used to specify the channel for the offset/gain adjustment. (Channel other than channels 1 to 4 is not processed.)
(3)	OFFSET switch OFFSET	Stores the analog input value in A1S64AD as an offset value by setting the switch to the OFFSET side.
(4)	GAIN switch GAIN	Stores the analog input value in A1S64AD as an offset value by setting the switch to the GAIN side.
(5)	Test mode terminals TEST	Connected between terminals No.1 and No.2 to set the offset/gain values.

3.5 Performance Specifications

3.5.1 A68AD

Item	Performance Specifications
Analog input	Selection depends on input terminals. Voltage: -10 to 0 to +10 VDC (Input resistance: 30 KΩ) Current: +4 to +20 mA DC (Input resistance: 250 Ω) *-20 to 0 to +20 mA can also be used for current input.
Digital output	A CPU: 16-bit, signed binary (-2048 to +2047)
I/O characteristics	**Analog Input** / **Digital Output** +10 V / +2000 +5 V or +20 mA / +1000 0 V or +4 mA / ±0 -5 V or -12 mA / -1000 -10 V / -2000
Maximum resolution	Voltage: 5 mV (1/2000) Current: 20 μA (1/1000)
Overall accuracy	Within: ±1 % (Accuracy with respect to the maximum value)
Maximum conversion speed	Maximum 2.5 ms/channel
Absolute maximum input	Voltage: ±15 V Current: ±30 mA
Number of analog input points	8 channels/unit
Insulation method	Photocoupler insulation between output terminals and PC power (Non-insulated between channels)
Number of I/O points	32 points
Connection terminal	38-point terminal block
Applicable wire size	0.75 to 2 mm^2 (Applicable tightening torque: 7 kg·cm)
Applicable solderless terminal	V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A
Internal current consumption (5 V)	0.9 A
Weight kg (lb)	0.6 (1.32)

(1) Differences between an A68AD and an A68AD-S2

Model Names / Differences	A68AD	A68AD-S2
Method of designating the channel by which A-D conversion is performed	Set the continuous number of channels beginning with channel 1.	Set the presence or absence of A-D conversion to every channel.
Timing of designating the channel by which A-D conversion is performed	Only once (at power ON)	Enabled even in the middle of A-D conversion is performed
A-D conversion-completed flag	None	The bits that correspond to B0 to B8 of buffer address 35 are ON.

(The User's Manual of the utilized module gives details.)

3.5.2 A0J2-68AD

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Analog input</td><td>Selection depends on input terminals.
Voltage: -10 to 0 to +10 VDC (Input resistance: 30 KΩ)
Current: +4 to +20 mA DC (Input resistance: 250 Ω)
* -20 to 0 to +20 mA can also be used for current input.</td></tr>
<tr><td>Digital output</td><td>A CPU: 16-bit, signed binary (-2048 to +2047)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th>Analog Input</th><th>Digital Output</th></tr>
<tr><td>+10 V</td><td>+2000</td></tr>
<tr><td>+5 V or +20 mA</td><td>+1000</td></tr>
<tr><td>0 V or +4 mA</td><td>±0</td></tr>
<tr><td>-5 V or -12 mA</td><td>-1000</td></tr>
<tr><td>-10 V</td><td>-2000</td></tr>
</table>
</td></tr>
<tr><td>Maximum resolution</td><td>Voltage: 5 mV (1/2000)
Current: 20 μA (1/1000)</td></tr>
<tr><td>Overall accuracy</td><td>Within ±1 % (Accuracy with respect to the maximum value)</td></tr>
<tr><td>Maximum conversion speed</td><td>Maximum 2.5 μs/channel</td></tr>
<tr><td>Absolute maximum input</td><td>Voltage: ±15 V
Current: ±30 mA</td></tr>
<tr><td>Number of analog input points</td><td>8 channels/unit</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulated between channels)</td></tr>
<tr><td>Number of I/O points</td><td>64 points</td></tr>
<tr><td>Connection terminal</td><td>36-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (Applicable tightening torque: 7 kg·cm)</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>Internal current consumption (5 V)</td><td>0.7 A</td></tr>
<tr><td>Weight kg (lb)</td><td>0.6 (1.32)</td></tr>
</table>

POINT

Analog input allowed for maximum resolution and overall accuracy, is from -10 to 0 to +10 V or from -20 to 0 to +20 mA.

3.5.3 A68ADC

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Analog input</td><td>Selection depends on input terminals.
Voltage: -10 to 0 to +10 VDC (Input resistance: 30 KΩ)
Current: +4 to +20 mA DC (Input resistance: 250 Ω)
* -20 to 0 to +20 mA can also be used for current input.</td></tr>
<tr><td>Digital output</td><td>16-bit, signed binary (11-bit data part) -2048 to +2047</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th>Analog Input</th><th>Digital Output</th></tr>
<tr><td>+10 V</td><td>+2000</td></tr>
<tr><td>+5 V or +20 mA</td><td>+1000</td></tr>
<tr><td>0 V or +4 mA</td><td>±0</td></tr>
<tr><td>-5 V or -12 mA</td><td>-1000</td></tr>
<tr><td>-10 V</td><td>-2000</td></tr>
</table>
</td></tr>
<tr><td>Maximum resolution</td><td>Voltage: 5 mV (1/2000) *1
Current: 20 μA (1/1000)</td></tr>
<tr><td>Overall accuracy</td><td>Within ±1 % (Accuracy with respect to the maximum value) *1</td></tr>
<tr><td>Maximum conversion speed</td><td>Maximum 2.5 ms/channel *2</td></tr>
<tr><td>Absolute maximum input</td><td>Voltage: ±15 V
Current: ±30 mA</td></tr>
<tr><td>Number of analog input points</td><td>8 channels/unit</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulated between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque: 7 kg·cm (6.06 lb·in.))</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.3 A</td></tr>
<tr><td>Weight kg (lb)</td><td>1.01 (2.22)</td></tr>
<tr><td>Outside dimensions mm (in.)</td><td>170 (6.69) (H) x 100 (3.94) (W) x 80 (3.15) (D)</td></tr>
</table>

POINTS

*1 Analog input allowed for maximum resolution and overall accuracy, is from -10 to 0 to +10 V or form -20 to 0 to +20 mA.

*2 The maximum conversion speed indicates that of a single A68ADC module. The time required for the PC CPU to read digital output after A/D conversion should be the maximum conversion speed plus the time required for communication with the A68ADC.

3.5.4 A1S64AD

Item	Specifications			
Analog input	Voltage: -10 to 0 to +10 VDC (Input resistance: 1 MΩ) Current: -20 to 0 to +20 mA (Input resistance: 250 Ω)] Selectable by input terminals			
Digital output	Signed 16 bit binary [1/4000: -4096 to 4095 1/8000: -8192 to 8191 1/12000: -12288 to 12287]			
I/O characteristics	**Analog input**	**Digital output (Gain: 5 V/20 mA, Offset: 0 V/0 mA)**		
		1/4000	**1/8000**	**1/12000**
	+10 V +5 V or +20 mA 0 V or 0 mA -5 V or -20 mA -10 V	+4000 +2000 0 -2000 -4000	+8000 +4000 0 -4000 -8000	+12000 +6000 0 -6000 -12000
Maximum resolution		1/4000	1/8000	1/12000
	Voltage input Current input	2.5 mV 10 μA	1.25 mV 5 μA	0.83 mV 3.33 μA
Overall accuracy	±1.0 % (Accuracy to the maximum value)			
Maximum conversion time	Maximum 20 msec/channel			
Absolute maximum output	Voltage: ±15 V Current: ± 30 mA			
Analog input points	4 channels/module			
Insulation method	Photocoupler insulation between input terminals and PC power (Non-insulation between channels)			
Number of I/O points	32 points			
Connection terminal	20-point terminal block			
External power supply	Not required			
Applicable wire size	0.75 to 1.5 mm^2			
Applicable solderless terminal	1.25-3, 1.25-YS3, V1.25-3, V1.25-YS3A			
Internal current consumption (5 V)	0.4 A			
Weight kg (lb)	0.25 (0.55)			
External dimensions mm (in.)	130 (5.12) (H) x 34.5 (1.36) (W) x 93.6 (3.69) (D)			

- The gain value is set to 5 V/20 mA and the offset value is set to 0 V/ 4 mA at factory.

POINT

The available analog input range for the maximum resolution and overall accuracy is as follows:

Voltage: -10 to 0 to +10 V
Current: -20 to 0 to +20 mA

3.6 Wiring Instructions

Protect external wiring against noise with the following precautions:

(1) Separate AC and DC wiring.

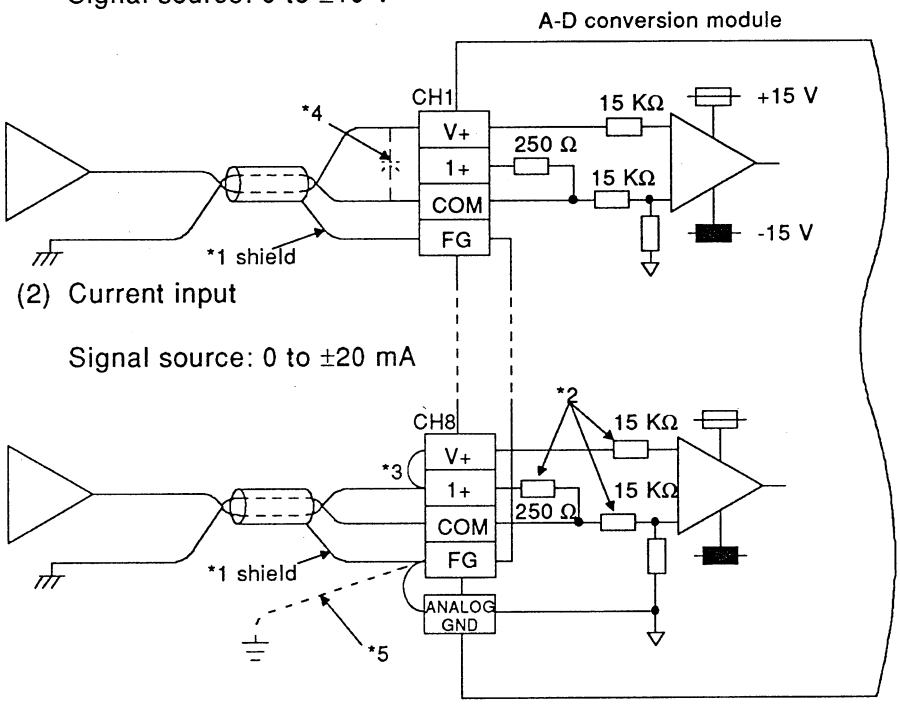
(2) Separate main circuit and/or high voltage wiring from conrol and signal wiring.

(3) Where applicable, ground the shielding of all wires to a common ground point.

3.7 Unit Connection Example

(1) Voltage input

Signal source: 0 to ±10 V



*1: For the cable, use a two-core twisted shielded wire.

*2: Indicates the input resistance of the A-D conversion module.

*3: For current input, be sure to connect the terminals (v+) and (1+).

*4: If noise or ripple is generated at the external wiring, connect a capacitor of approximately 0.1 to 0.47 μF25WV between terminals V and COM.

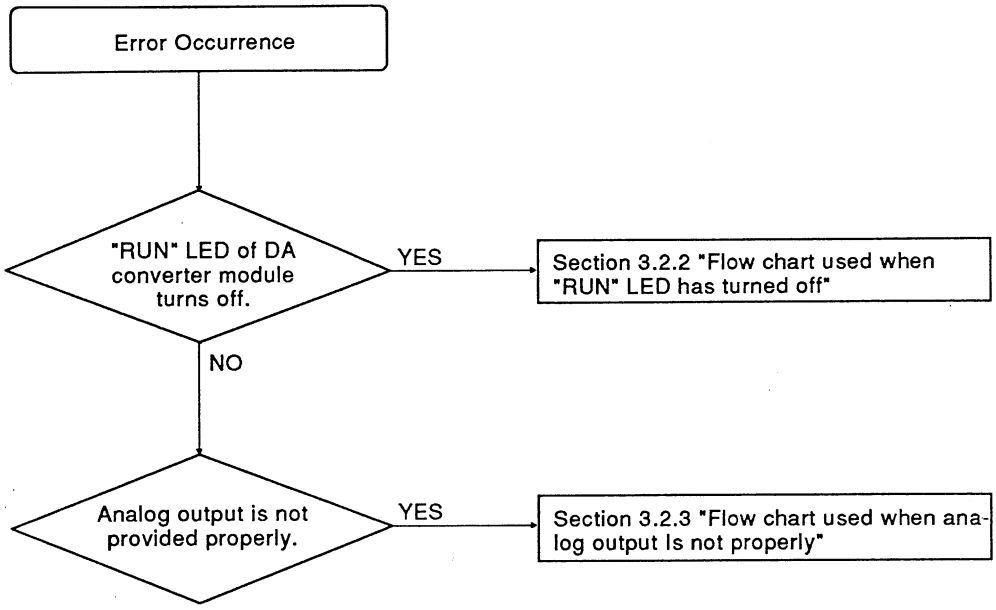
*5: If there is excessive noise, ground the unit.

POINT

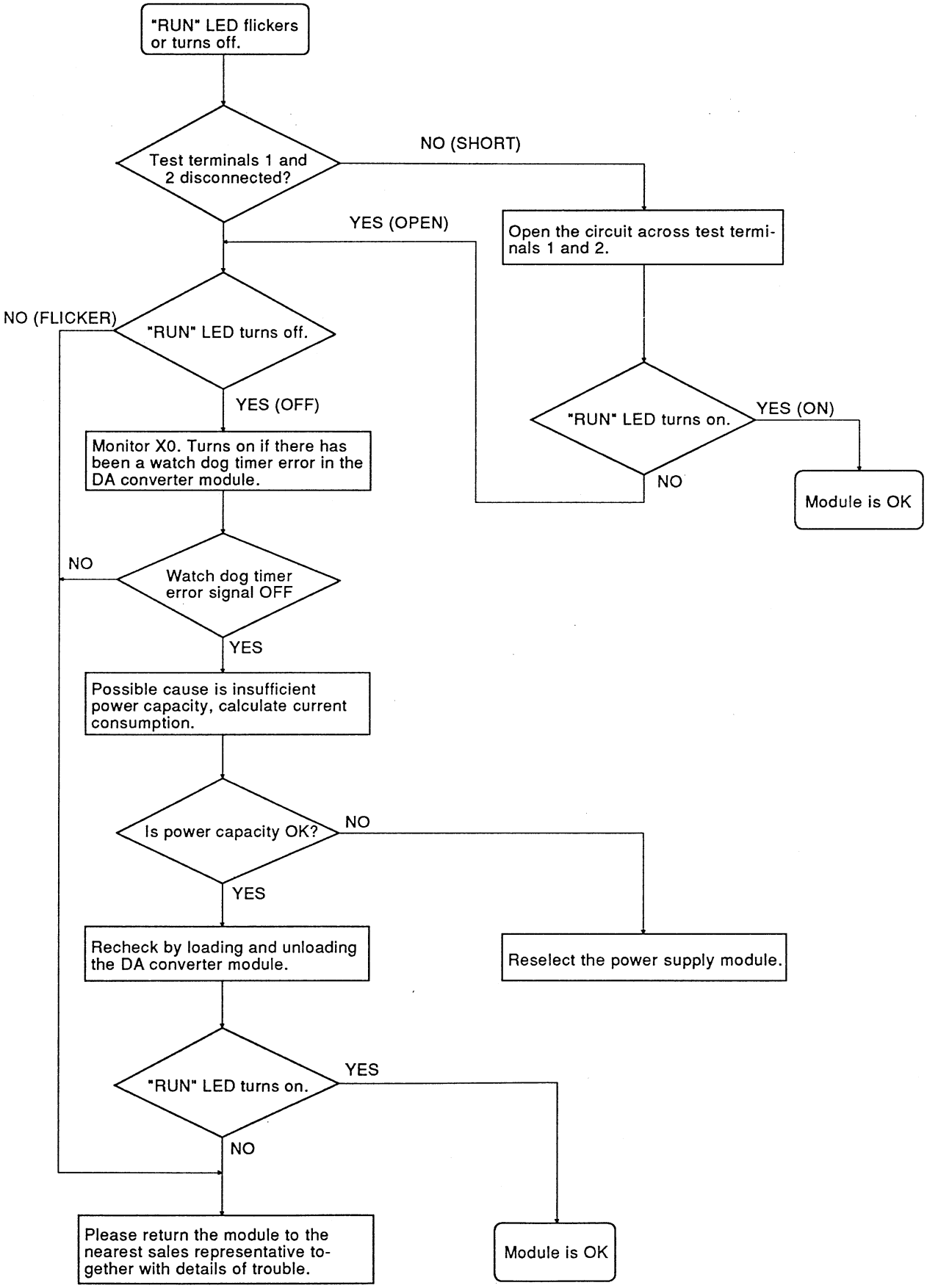
The FG terminal of the A-D conversion module and the FG terminal of the power supply unit are not connected together internally.

3.8 A0J2-62DA and A62DA Digital-to-Analog Conversion Modules

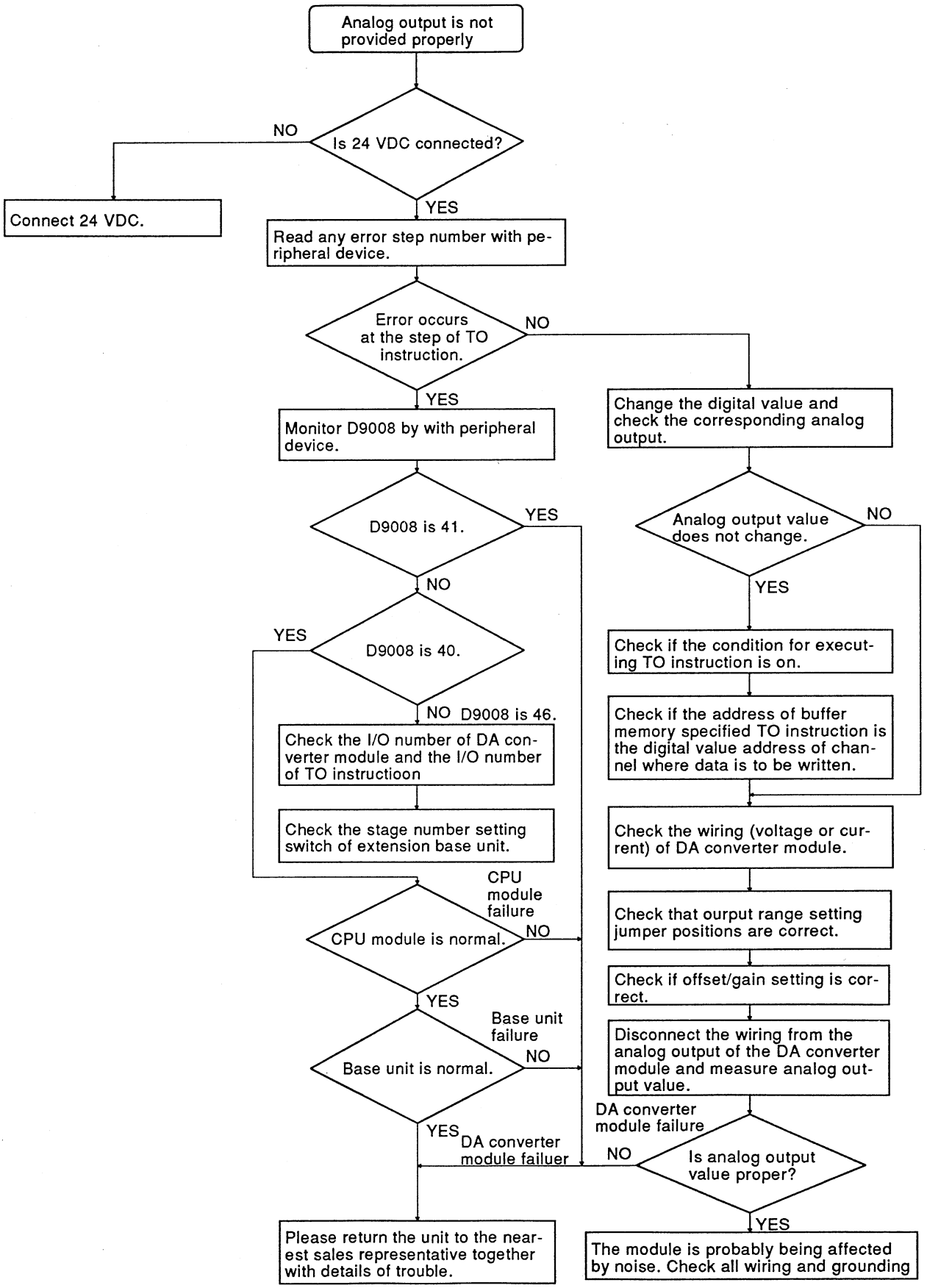
3.8.1 Troubleshooting flow chart



3.8.2 Flow chart used when "RUN" LED has flickered or turned off



3.8.3 Flow chart used when analog output is not provided properly



REMARK

The following contents are written into D9008 when an error has occurred during execution of the FROM or TO instruction.

Content (BIN value) of Special Register D9008	Error Message	CPU Status	Error and Cause
40	CONTROL-BUS ERR	Stop	FROM and TO instructions cannot be executed. Hardware failure of AD converter module (special function module), CPU unit, or base unit.
41	S.P UNIT DOWN	Stop	When the FROM or TO instruction has been executed, access has been made to the special function module but no answer is returned. The accessed AD converter module (special function module) has failed.
46	S.P UNIT ERROR	Stop (Continuous operation can be performed by the setting of parameter.)	Access has been made (FROM or TO instruction has been executed) to a slot where the AD converter module (special function module) is not loaded. The content of FROM or TO instruction is incorrect or the stage number setting of extension base unit is improper.

3.9 A64DAVC/DAIC Digital-to-Analog Conversion Unit

3.9.1 Error code list

(1) If an error has occurred when data is written to the A64DAVC/DAIC (the RUN LED fickers), any of the error codes mentioned in the list below is stored in buffer memory at address 9. When the A2CCPU is used, the same error code is stored also in special registers D9180 to D9193. When the AJ71PT32-S3 is used, the same error code is stored also in buffer memory at addresses 196 to 209.

Error Code	Cause	Corrctime Action
100 (64_H)	(Read error) • Designated head address is out of buffer memory. • Designated range of read words includes addresses out of buffer memory.	Correct data which designates range out of buffer memory.
101 (65_H)	(Write error) • Designated head address is out of buffer memory. • Designated range of write words includes addresses out of bueffer memory. • Write was attempted to read-only areas.	• Correct data whichh designates range out of buffer memory. • Correct data which designates range read-only areas.
102 (66_H)	Command code other than read (1) or wirte (2) is received.	May be influenced by noise. Take measures against noise.
103 (67_H)	Data was received immediately after read command (1).	
104 (68_H)	Read and write word length is set at "0".	
105 (69_H)	The number of words set by write command data differs from that of received data.	
11 [ ]	Digital values were set out of the specified range. [ ] indicates the channel on which the error occurred.	Correct digital values into the specified range.
12 [ ]	Analog output enable/disable setting was done with other than 0 or 1. [ ] indicates the channel on which the error occurred.	Correct analog output enable/disable setting to 1 (enable) or 0 (disable).
130	Digital value resolution was set with other than 1, 2 or 3.	Correct digital value resolution setting to 1 (1/4000), 2 (1/8000) or 3 (1/12000).

(a) If two or more errors occur continuously, the error code for the first error is stored, and following error codes are not stored.

(b) Error code reset is done by writing "0" to address 18 of buffer memory. (Figures other than 0 are ignored.)

(2) When the AJ71PT32-S3 is used, error codes for the errors occur during communication with remote terminal modules are stored in buffer memory at addresses 196 to 209 in addition to the error codes for errors detected by the A64DAVC/DAIC.

Error Code	Error Name	Cause	Corrective Action
1	Set data error	Data written to the remote terminal transmission areas includes errors.	Correct the data.
6	WDT error	Remote terminal module malfunction.	• Reset faulty remote terminal module. • Turn OFF and then ON the power. • If the above procedures do not recover the system, the system hardware is faulty. Please consult Mitsubishi representative.
8	Transmission area setting error	Remote terminal transmission area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.
9	Communication error	Communication between the master module and remote terminal modules is faulty.	Noise or remote terminal module failure.
11 (A_H)			
10 (A_H)	Receive area setting error	Remote terminal receive area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.

3.9.2 When the RUN LED flickers or turned OFF

(1) When flickers:

Check Point	Correctibe Action
Data which disables write or read is written to the A64DAVC/DAIC.	• Refer to the List of Error Codes (Section 3.9.1) for the cause, and correct the sequence program. • Check the transmission system and influence of noise.
The TEST terminals are shorted. (Test mode)	Perform offset/gain adjustment, and then, open the TEST terminals.
The LED is flickering at 0.1 sec intervals in test mode.	Perform offset/gain adjustment in the specified range.

(2) When turned OFF:

Check Point	Corrective Action
24 VDC power supply is turned on.	Make sure the power supply.
24 VDC power supply voltage is within the set range.	Adjust the voltage within 15.6 to 31.2 V range.
If the MINI-S3 link is connected, the MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Add a loop to turn ON the MINI-S3 link communication start signal $Y_{(n+28)}$ to the sequence program.
If the MINI-S3 link is connected, error code "6" may be stored in the master module buffer memory at address 196 to 209.	Reset the PC CPU, and start them in the same manner. If error code "6" is again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
If the MINI-S3 link is connected, error codes "9" and "10" may be stored in the master module buffer memory at address 196 to 209.	Reset the PC CPU, and start them in the same manner. If error codes "9" and "10" are again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
Data link cables are normal.	Check the cables.
The TEST terminals are shorted. (Test mode)	After offset/gain setting, open the TEST terminals.

3.9.3 When the LINK RUN LED turned OFF or the LINK ERR. LED turned ON

Check Point	Corrective Action
The RUN LED is flickering.	Follow Section 3.9.2 (1).
The RUN LED turned OFF.	Follow Section 3.9.2 (2).

3.9.4 When analog output is not provided correctly

Check Point		Corrective Action
The RUN LED is flickering or turned OFF.		Follow Section 3.9.2.
The ERROR LED of the CPU module is flickering or turned ON.		Refer to the User's Manual for respective CPU module for error content.
The RUN LED of the CPU module is flickering or turned OFF.		Refer to the User's Manual for respective CPU module for error content.
When A2CCPU is used:	The RD/SD LED of the CPU module is flickering. (normal)	Refer to the A2CCPU User's Manual for error content.
When AJ71PT32-S3 is used:	The MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Set the sequence program to turn ON the MINI-S3 link communication start signal.
	The RUN LED of the master module is turned OFF.	Refer to the AJ71PT32-S3 User's Manual for error content.
	The RD/SD LED of the master module is flickering. (normal)	Refer to the AJ71PT32-S3 User's Manual for error content.
Analog input signal lines are broken or disconnected. Locate trouble by checking the signal lines visually and for continuity. Disconnect the wiring from the analog output of the A64DAVC/DAIC and measure analog output at the module terminals.		• If analog output measured at the module terminals is correct, the external wiring may be broken or affected by noise. Check all wiring and grounding. • Separate the module from the frame and disconnect the grounding circuit. (Mount the module to the DIN rail.)

3.10 A1S62DA Degital-to-Analog Conversion Module

3.10.1 When the RUN LED flashes or goes OFF

(1) When the RUN LED goes OFF:

Items to Check	Corrective Actions
Are the TEST terminals shorted? (Test mode)	Make offset/gain adjustments, and then open the TEST terminals.
Has an error occurred in the CPU module?	Refer to the appropriate User's Manual for error information, and correct the error.
Is the power supply module (5 VDC) that is installed to the base unit not getting enough current?	Recalculate the total number of amps for the CPU, I/O module, and special function module installed to the base unit, and replace the power supply module if necessary.
Is the A1S62DA WDT error flag set?	Reset the CPU module.

(2) When the RUN LED flashes:

Items to Check	Corrective Actions
Are the TEST terminals shorted when offset/gain select switch is set to OFFSET or GAIN? (Test mode)	Set the offset/gain, and then open the TEST terminals.
Does the LED flash at one-tenth (0.10) of a second intervals when in the test mode?	Reset the CPU module.
Is the digital value outside the setting range written?	Clear the setting value check code storage area with an error reset flag.

3.10.2 When the analog value is 0 V/0 mA

(1) When the values of all channels are 0 V/0 mA:

Items to Check	Corrective Actions
Is the RUN LED of the A1S62DA turned OFF?	Follow procedures in Section 3.10.1.
Are the analog output enable/disable channels of each channel set to disable?	Set the analog output enable/disable of the channels to be used to enable.
Is the WDT error flag set?	Follow procedures in Section 3.10.7.
Is the D-A conversion ready flag set?	Follow procedures in Section 3.10.8.
Is the digital value written in the digital value setting area (addresses 1 and 2) of the buffer memory?	Write the digital values of the channel to be converted from digital to analog.

(2) When the value of a given channel is 0 V/0 mA:

Items to Check	Corrective Actions
Is the analog output enable/disable channel with its "0 V/0 mA" analog value set to disable?	Confirm the data set in the analog output enable/disable channel setting area of the buffer memory.
Is the digital value of the channel with its "0 V/0 mA" analog value written in the digital value setting area of the buffer memory?	Write the digital value.
Is the external wiring done correctly?	Make sure the external wiring is correct.

3.10.3 When analog values are offset values

(1) When the analog values of all channels are offset values:

Items to Check	Corrective Actions
Are the TEST terminals shorted? (Test mode)	Make offset/gain adjustments, and then open the TEST terminals.
Is the RUN key switch of the CPU module set to a position other than "RUN"?	Set the switch to the RUN position.
Are the D-A conversion value output enable flags of each channel reset?	Set the D-A conversion value output flags of the channels to be used.
Is the digital value written in the digital value setting area (addresses 1 and 2) of the buffer memory?	Write the digital values of the channel to be converted from digital to analog.

(2) When the analog value of a given channel is an offset value:

Items to Check	Corrective Actions
Is the D-A conversion value output enable flag setting for a channel whose analog value is an offset value reset?	Set the D-A conversion value output enable flag.
Is the digital value of the channel whose analog value is an offset value written to the digital value setting area of the buffer memory?	Write the digital value.

3.10.4 Analog values are output although the CPU module is set to STOP

(1) When the analog output does not change after setting to STOP.

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted (held)? • Is the D-A conversion value output enable flag of the channel outputting analog values set to enable? • Is the enable/disable output of the channel outputting analog values set to enable?	If one or more of these conditions exist, make the necessary corrections.

(2) When the analog output changes after setting to STOP:

Items to Check	Corrective Actions
Is the outputted analog value offset value?	Confirm the offset value. When making the output value 0 V/0 mA, set the offset again.

3.10.5 When analog values output although the output enable flag (Y10 and Y11) is reset

(1) When offset values are output:

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted (held)? • Is the D-A conversion value output enable flag of the channel outputting offset values set to disable? • Are the HOLD/CLEAR setting terminals shorted (HOLD)? • Is the analog output enable/disable channel for outputting analog values set to enable? • Is the digital value not set to "0"?	If one or more of these conditions exist, make the necessary corrections.

(2) When analog values (except offset values) are output:

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted(held)? • Are the HOLD/CLEAR setting terminals of analog output shorted (HOLD)? • Is the D-A conversion value output enable flag of the channel outputting analog values set to enable? • Is the analog output enable/disable channel for outputting analog values set to enable? • Is the digital value not set to "0"?	If one or more of these conditions exist, make the necessary corrections.

3.10.6 When digital and analog values do not match

(1) When both digital values and analog values change:

Items to Check	Corrective Actions
Does the digital value match the analog value?	Correct the offset/gain values.
Are the A1S62DA and external devices properly wired?	Make sure the wiring between the A1S62DA and the external devices is correct.
Is the digital values written in the digital setting area (addresses 1 and 2) incorrect?	Write the proper values to the addresses of the corresponding channels in the buffer memory.

(2) When the digital value changes and the analog value is fixed:

Items to Check	Corrective Actions
Is the RUN key switch of the CPU module set to a position other than "RUN"?	Set the switch to the RUN position
Is the digital value written in the digital value setting area of the buffer memory (addresses 1 and 2)?	Write the digital value of the channel to be converted from digital to analog.

3.10.7 WDT error flag (X0) is set

Items to Check	Corrective Actions
When the CPU module is reset, is the WDT error flag reset?	Check to see if there is a transmission error, and if the CPU module is affected by noise.

3.10.8 D-A conversion READY flag (X1) is reset

Items to Check	Corrective Actions
Is there an error in the CPU module?	See the corresponding User's Manual for the respective CPU module for error information. Correct the error.
Is there an I/O number error?	Confirm and correct the I/O number.
Are the TEST terminals shorted? (Test mode)	Open the TEST terminals and cancel the test mode.

3.10.9 Error flag (X2) is set

Items to Check	Corrective Actions
Is a value that is not "0" set in the setting value check code storage area (addresses 10 and 11) of the buffer memory?	Verify that a digital value outside the setting range was written in which data other that "0" is stored to a channel and its corresponding check code storage area. Clear the set value storage area with the error reset flag (Y18).

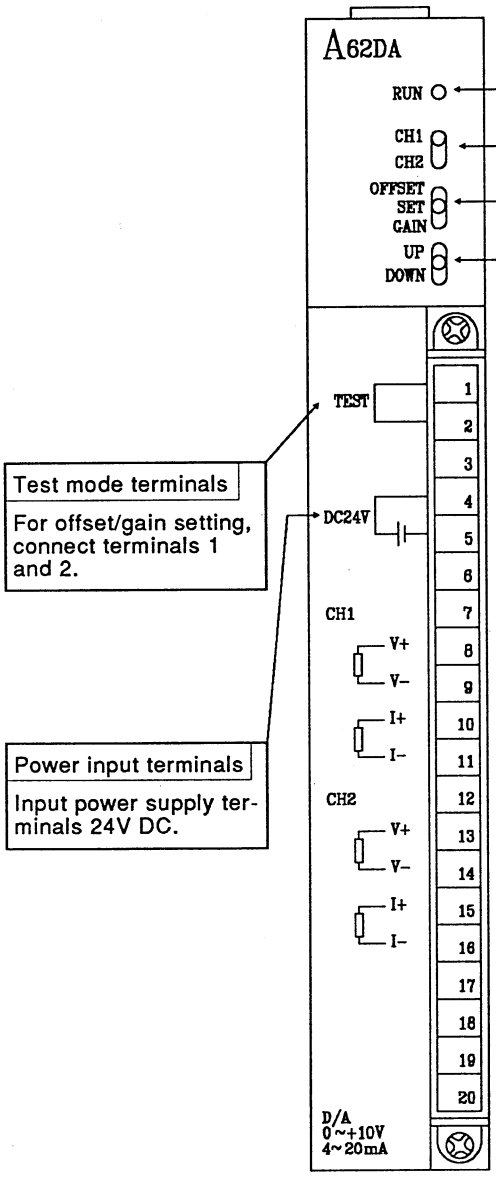
POINT

If these corrective measures do not solve the problem, there may be a hardware malfunction in the module.

Consult a Mitsubishi representative.

3.11 Nomenclature

3.11.1 A62DA



RUN LED

Indicates the operating status of A62DA.
(Normal mode)
ON: During normal operation
OFF: 5 V power off or watch dog timer error
(Test mode)
Flicker: Flickers at intervals of 0.25s when the OFFSET/GAIN select switch is located at the OFFSET or GAIN position. Flickers at high speed at intervals of 0.1s when the setting range (refer to Section 6.1) has been exceeded and the upper limit value or lower limit value has been reached.
OFF: When both the OFFSET/GAIN select switch is located at the SET position.

Test mode terminals

For offset/gain setting, connect terminals 1 and 2.

***CHANNEL select switch**

Used to select a channel for the adjustment of offset value and gain value.

Power input terminals

Input power supply terminals 24V DC.

***OFFSET/GAIN select switch**

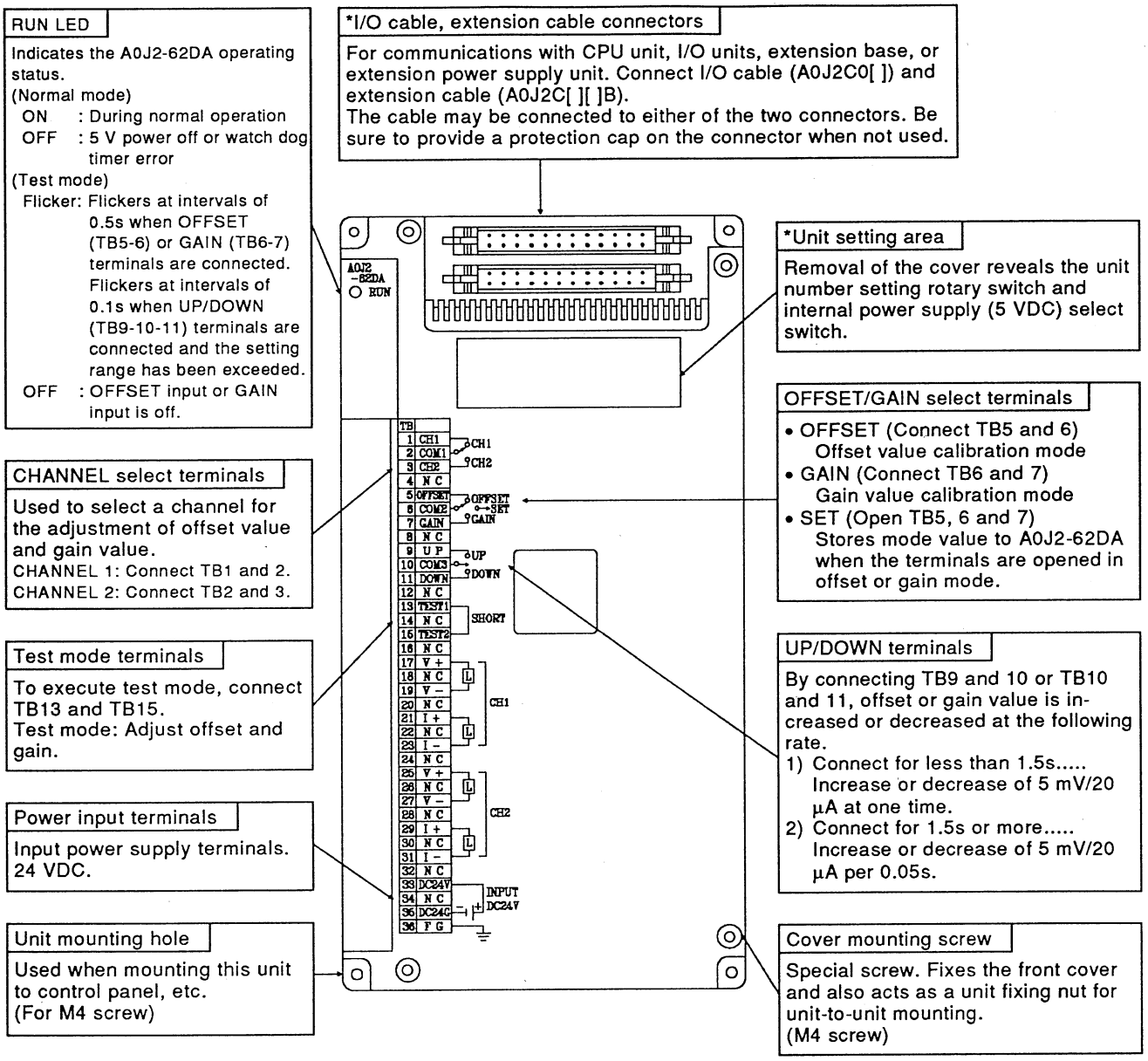
OFFSET posetion: Offset value calibration mode
GAIN position: Gain value calibration mode
SET position: When the switch is moved from the OFFSET or GAIN position to the SET position, an offset value or a gain value is stored into A62DA.

***UP/DOWN switch**

Used to increase or decrease the offset value or gain value of specified channel at the following rate:
1) On less than 1.5 seconds:
In increments or decrements of 1.25 mV (0 to 5 V mode)
1 mV (1 to 5 V mode)
2.5 mV (0 to 10 V mode)
5 μA (0 to 20 mA mode)
or 4 μA (4 to 20 mA mode)
at one time.
2) On 1.5 seconds or longer:
In increments or decrements of 1.25 mV (0 to 5 V mode)
1 mV (1 to 5 V mode)
2.5 mV (0 to 10 V mode)
5 μA (0 to 20 mA mode)
or 4 μA (4 to 20 mA mode)
per 0.05 seconds.

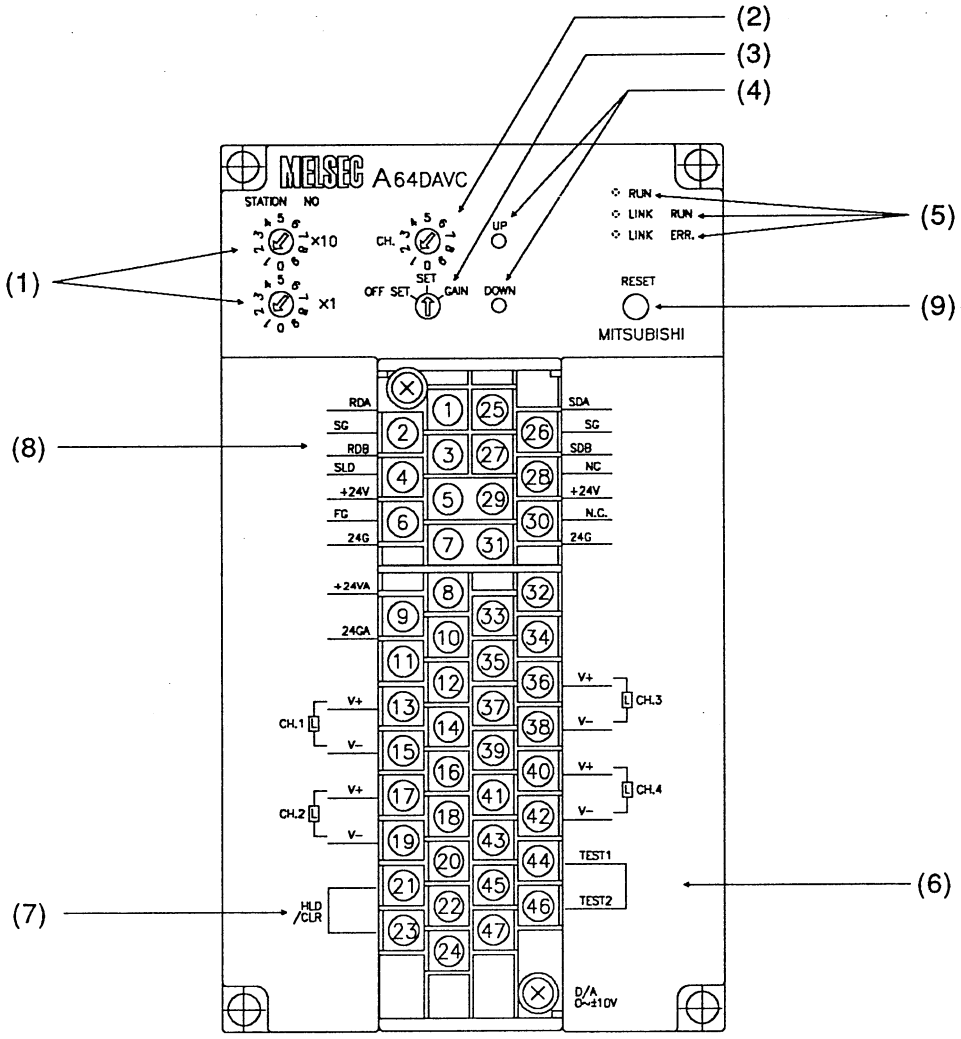
Switches marked * are valid only in test mode.

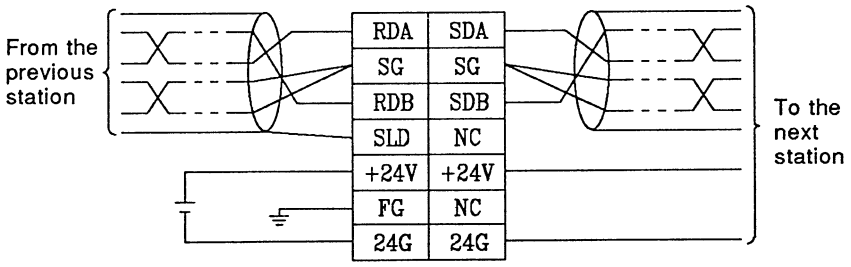
3.11.2 A0J2-62DA



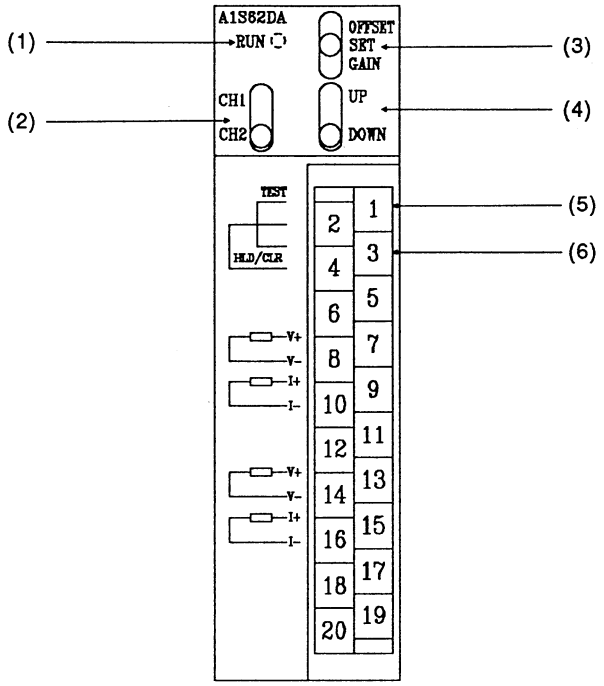
It is necessary to set the area in * prior to test operation and adjustments.

3.11.3 A64DAVC/DAIC

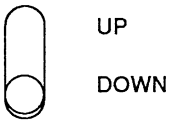
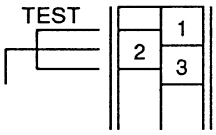
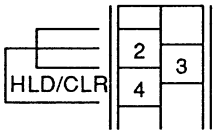


<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>(1)</td><td>Station number setting switches</td><td>(↓) x 10 ┐ Used to set the station number of the A64DAVC/DAIC in a range
(↓) x 1 ┘ from 1 to (64 - occupied stations + 1).</td></tr>
<tr><td>(2)</td><td>Channel select switch</td><td>Used to select the channel for offset/gain adjustment.
(Positions 0 and 9 select no processing.)</td></tr>
<tr><td>(3)</td><td>OFFSET/GAIN setting switch</td><td>Used to set offset/gain values in test mode.
(1) OFFSET: Offset value calibration
(2) GAIN: Gain value calibration
(3) SET: Offset/gain value storage
(Analog output when this switch is turned from OFFSET/GAIN to SET is stored as offset/gain value in the internal memory of the A64DAVC/DAIC.)</td></tr>
<tr><td>(4)</td><td>UP/DOWN switches</td><td>Used to adjust analog output of offset/gain of specified channel. Turning ON the UP/DOWN switches makes analog output increase/decrease.</td></tr>
<tr><td>(5)</td><td>Operation state indicator LEDs</td><td>
<table>
<tr><td rowspan="2">RUN</td><td>Normal mode</td><td>On: Normally running
Flicker: Read/write data error
Off: 24 VDC is off or WDT error.</td></tr>
<tr><td>Test mode</td><td>Flicker: Flickers at 0.5 sec intervals when the OFFSET/GAIN switch is in the OFFSET or GAIN position. Flickers at 0.1 sec intervals when analog output exceeded the upper or lower limit of the setting range when the UP/DOWN switches are used.
Off: When the OFFSET/GAIN switch is in the SET position.</td></tr>
<tr><td>LINK RUN</td><td>On:
Off:</td><td>Normal communication
Receive data error</td></tr>
<tr><td>LINK ERR</td><td>On:
Off:</td><td>Receive data error
Normal communication</td></tr>
</table>
</td></tr>
<tr><td>(6)</td><td>Test mode terminals</td><td>Shorted when setting offset/gain.</td></tr>
<tr><td>(7)</td><td>Analog output HOLD/CLEAR setting terminals</td><td>(1) HOLD setting: short the terminals.
(2) CLEAR setting: Open the terminals.</td></tr>
<tr><td>(8)</td><td>Terminal block for twisted pair cables and power supply cables</td><td> 
</td></tr>
<tr><td>(9)</td><td>Rest switch</td><td>Hardware reset
Used to initialize buffer memory and operation processing of the A64DAVC/DAIC.
By turning this ON, the control input signal X5 of the A64DAVC/DAIC turns ON.
(Device number of control I/O signals depends on station setting.)</td></tr>
</table>

3.11.4 A1S62DA



No.	Description	Application
(1)	"RUN" LED	Indicates the operating status of the A1S62DA. (Normal mode) On: Indicates that the A1S62AD is operating without fault. Off: External power 5 VDC is not supplied to the A1S62DA or A1S62DA is in WDT error Flash: When the digital value is written beyond the high ot low limit, this LED flashes every second. (Test mode) Off: OFFSET/GAIN select switches is inthe "SET" position. Flash: When the offset/gain select switch is set to either the OFFSET or GAIN position, this LED flashes every half (0.5) second. When the UP/DOWN switch is set to the upper or lower limit of a setting range, this LED flashes every tenth (0.10) of a second.
(2)	Channel select switch CH1 CH2	Used to specify the channel for the offset/gain adjustment.
(3)	OFFSET/GAIN switch OFFSET SET GAIN	OFFSET position : Sets the offset value. GAIN position : Sets the gain value. SET position : The offset/gain value is stored to the A1S62DA internal memory when the switch is moved from "OFFSET"/"GAIN" to "SET".

No.	Description	Application
(4)	GAIN switch 	Increase or decreases the offset/gain value for the specified channel.
(5)	Test mode terminals 	Connected between terminals No.1 and No.3 to set the offset/gain values.
(6)	Output HOLD/CLEAR setting terminals 	Used to hold or clear the analog output at the time of CPU STOP. Disconnected between terminal No.2 and No.4: CLEAR Connected between terminal No.2 and No.4: HOLD

3.12 Performance Specifications

3.12.1 A62DA

<table>
<tr><th colspan="2">Item</th><th>Specifications</th></tr>
<tr><td colspan="2">Digital input</td><td>Max. setting value
Voltage: ±2000
Current: ±1000</td></tr>
<tr><td colspan="2">Analog output</td><td>Voltage: -0 to +10 VDC
(External load resistance: 500 Ω to 1 MΩ)
Current: +4 to +20 mA can also be used for current output.
(External load resistance: 0 Ω to 600 Ω)</td></tr>
<tr><td colspan="2">I/O characteristics</td><td>
<table>
<tr><th rowspan="2">Digital input</th><th colspan="2">Analog output</th></tr>
<tr><th>Voltage</th><th>Current</th></tr>
<tr><td>+2000</td><td>+10 V</td><td>—</td></tr>
<tr><td>+1000</td><td>+5 V</td><td>+20 mA</td></tr>
<tr><td>0</td><td>0 V</td><td>+4 mA</td></tr>
<tr><td>-1000</td><td>-5 V</td><td>-12 mA</td></tr>
<tr><td>-2000</td><td>-10 V</td><td>—</td></tr>
</table>
</td></tr>
<tr><td rowspan="2">Maximum resolution</td><td>Voltage</td><td>5 mV (1/2000)</td></tr>
<tr><td>Current</td><td>20 μA (1/1000)</td></tr>
<tr><td colspan="2">Over accuracy
(Accuracy for max. value)</td><td>±1 %</td></tr>
<tr><td colspan="2">Maximum conversion speed</td><td>Within 15 ms/2 channels (Time for 1 channel is also the same.)
Note: Time period between digital input write and specified analog voltage (current) reached.</td></tr>
<tr><td colspan="2">Absolute maximum output</td><td>Voltage: 0 to +12 V
Current: 0 to +28 mA
Note: Max. output voltage and current restricted by output protection circuit.</td></tr>
<tr><td colspan="2">Number of analog output points</td><td>2 channels/module</td></tr>
<tr><td colspan="2">Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulated between channels)</td></tr>
<tr><td colspan="2">Number of I/O occupying points</td><td>32 points</td></tr>
<tr><td colspan="2">Connection terminal</td><td>20-point terminal block</td></tr>
<tr><td colspan="2">Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque: 7 kg·cm (6.06 lb·in.))</td></tr>
<tr><td colspan="2">Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td colspan="2">Internal current consumption
(5 V)</td><td>0.6 A</td></tr>
<tr><td rowspan="2">External supply power</td><td>Voltage</td><td>21.6 to 26.4 VDC</td></tr>
<tr><td>Current consumption</td><td>0.35 A (at 24 VDC)</td></tr>
<tr><td colspan="2">Weight kg (lb)</td><td>0.5 (1.1)</td></tr>
</table>

POINT

The analog output ranges for maximum resolution and maximum over-all accurary, is from -10 to 0 to +10 V or from -20 to 0 to +20 mA.

3.12.2 A0J2-62DA

<table>
<tr><th colspan="2">Item</th><th>Sepecifications</th></tr>
<tr><td colspan="2">Digital input</td><td>Voltage output, digital setting range: ±2000
Current output, digital setting range: ±1000</td></tr>
<tr><td colspan="2">Analog output</td><td>Selectively used depending on output terminals.
Voltage: -10 to 0 to +10 VDC
(External load resistance: 500 Ω to 1 MΩ)
Current: +4 to +20 mA DC
(External load resistance: 0 Ω to 600 Ω)
*-20 to 0 to +20 mA can also be used for current output.</td></tr>
<tr><td colspan="2">I/O characteristics</td><td>
<table>
<tr><th rowspan="2">Digital Input</th><th colspan="2">Analog Output</th></tr>
<tr><th>Voltage</th><th>Current</th></tr>
<tr><td>+2000</td><td>+10 V</td><td>—</td></tr>
<tr><td>+1000</td><td>+5 V</td><td>+20 mA</td></tr>
<tr><td>0</td><td>0 V</td><td>+4 mA</td></tr>
<tr><td>-1000</td><td>-5 V</td><td>-12 mA</td></tr>
<tr><td>-2000</td><td>-10 V</td><td>—</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Maximum resolution</td><td>Voltage: 5 mA (1/2000)
Current: 20 μA (1/1000)</td></tr>
<tr><td colspan="2">Overall accuracy</td><td>Within ±1 % (Accuracy with respect to the maximum value)</td></tr>
<tr><td colspan="2">Maximum conversion speed</td><td>Within 16 ms/2 channels (Time for 1 channel is also the same.)
Note: Time from when digital input is written to when analog voltage (current) changes from -10 V (-20 mA) to +10 V (+20 mA).</td></tr>
<tr><td colspan="2">Absolute maximum output</td><td>Voltage: ±12 V
Current: ±28 mA
Note: Max. output voltage and current restricted by output protection circuit.</td></tr>
<tr><td colspan="2">Number of analog output points</td><td>2 channels/unit</td></tr>
<tr><td colspan="2">Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulated between channles)</td></tr>
<tr><td colspan="2">Number of I/O occupying points</td><td>64 points</td></tr>
<tr><td colspan="2">Connection terminal</td><td>36-point terminal block</td></tr>
<tr><td colspan="2">Applicable wire size</td><td>0.75 to 2 mm^2 (Applicable tightening torque: 7 kg·cm)</td></tr>
<tr><td colspan="2">Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td colspan="2">Internal current consumption (5 V)</td><td>0.55 A</td></tr>
<tr><td rowspan="3">External supply power</td><td>Voltage</td><td>21.6 to 26.4 VDC</td></tr>
<tr><td>Current consumption</td><td>0.23 A (at 24 VDC)</td></tr>
<tr><td>Inrush current</td><td>0.6 A, 100 ms (24 VDC)</td></tr>
<tr><td colspan="2">Weight kg (lb)</td><td>0.75 (1.65)</td></tr>
</table>

3.12.3 A64DAVC

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Digital output</td><td>(1) 16-bit signed binary data
(2) Setting range:
<table>
<tr><th>Resolution Setting</th><th>Setting range</th></tr>
<tr><td>1/4000</td><td>-4096 to 4095</td></tr>
<tr><td>1/8000</td><td>-8192 to 8191</td></tr>
<tr><td>1/12000</td><td>-12288 to 12287</td></tr>
</table></td></tr>
<tr><td>Analog input</td><td>-10 to 0 to 10 VDC
(External load resistance: 2 KΩ to 1 MΩ)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th rowspan="2">Digital input value</th><th colspan="3">Digital Value Resolution</th><th rowspan="2">Analog Output *</th></tr>
<tr><th>1/4000</th><th>1/8000</th><th>1/12000</th></tr>
<tr><td>4000</td><td>8000</td><td>12000</td><td>+10 V</td></tr>
<tr><td>2000</td><td>4000</td><td>6000</td><td>+5 V</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0 V</td></tr>
<tr><td>-2000</td><td>-4000</td><td>-6000</td><td>-5 V</td></tr>
<tr><td>-4000</td><td>-8000</td><td>-12000</td><td>-10 V</td></tr>
</table>
* When offset setting is 0 V and gain setting is 10 V.</td></tr>
<tr><td>Maximum resolution of digital value</td><td>1/4000, 1/8000, 1/12000</td></tr>
<tr><td>Overall accuracy</td><td>±1.0 %</td></tr>
<tr><td>Maximum conversion speed</td><td>Maximum 25 msec/4 channels (same for 1 channel)
Note: Time from input of digital value till specified analog value (voltage) is output.</td></tr>
<tr><td>Analog output points</td><td>4 channels/module</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulation between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque: 7 kg·cm (6.06 lb·in.)</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.12 A</td></tr>
<tr><td>Weight kg (lb)</td><td>1.01 (2.22)</td></tr>
<tr><td>Outside dimensions mm (in.)</td><td>170 (6.69) (H) x 100 (3.94) (W) x 80 (3.15) (D)</td></tr>
</table>

3.12.4 A64DAIC

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Digital output</td><td>(1) 16-bit signed binary data
(2) Setting range:
<table>
<tr><th>Resolution Setting</th><th>Setting range</th></tr>
<tr><td>1/4000</td><td>0 to 4095</td></tr>
<tr><td>1/8000</td><td>0 to 8191</td></tr>
<tr><td>1/12000</td><td>0 to 12287</td></tr>
</table></td></tr>
<tr><td>Analog input</td><td>0 DC to 20 mA
(External load resistance: 0 to 600 Ω)</td></tr>
<tr><td>I/O characteristics</td><td>
<table>
<tr><th rowspan="2"></th><th colspan="3">Digital Value Resolution</th><th rowspan="2">Analog Output *</th></tr>
<tr><th>1/4000</th><th>1/8000</th><th>1/12000</th></tr>
<tr><td rowspan="3">Digital input value</td><td>4000</td><td>8000</td><td>12000</td><td>+20 mA</td></tr>
<tr><td>2000</td><td>4000</td><td>6000</td><td>+12 mA</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>+4 mA</td></tr>
</table>
* When offset setting is 4 mA and gain setting is 20 mA.</td></tr>
<tr><td>Maximum resolution of digital value</td><td>1/4000, 1/8000, 1/12000</td></tr>
<tr><td>Overall accuracy</td><td>±1.0 %</td></tr>
<tr><td>Maximum conversion speed</td><td>Maximum 25 msec/4 channels (same for 1 channel)
Note: Time from input of digital value till specified analog value (current) is output.</td></tr>
<tr><td>Analog output points</td><td>4 channels/module</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PC power
(Non-insulation between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque: 7 kg·cm (6.06 lb·in.)</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.15 A</td></tr>
<tr><td>Weight kg (lb)</td><td>1.01 (2.22)</td></tr>
<tr><td>Outside dimensions mm (in.)</td><td>170 (6.69) (H) x 100 (3.94) (W) x 80 (3.15) (D)</td></tr>
</table>

3.12.5 A1S62DA

<table>
<tr><th colspan="2" rowspan="2">Item</th><th colspan="6">Specifications</th></tr>
<tr><th colspan="4">Voltage Output</th><th colspan="3">Current Output</th></tr>
<tr><td>Digital input</td><td>1/4000
1/8000
1/12000</td><td colspan="4">-4000 to 4000
-8000 to 8000
-12000 to 12000</td><td colspan="3">0 to 4000
0 to 8000
0 to 12000</td></tr>
<tr><td colspan="2">Analog output</td><td colspan="4">-10 to 0 to 10 VDC
(External load resistance: 2 KΩ to 1 MΩ)</td><td colspan="3">0 to 20 mADC
(External load resistance: 0 to 600 Ω)</td></tr>
<tr><td rowspan="2">I/O characteristics</td><td>Resolution</td><td colspan="3">1/4000 1/8000 1/12000</td><td>Analog output value *1</td><td colspan="2">1/4000 1/8000 1/12000</td><td>Analog output value *2</td></tr>
<tr><td>Digtital input value</td><td colspan="3">4000 8000 12000
2000 4000 6000
0 0 0
-2000 -4000 -6000
-4000 -8000 -12000</td><td>10 V
5 V
0 V
-5 V
-10 V</td><td colspan="2">4000 8000 12000
2000 4000 6000
0 0 0</td><td>20 mA
12 mA
4 mA</td></tr>
<tr><td>Maximum resolution of analog value</td><td>1/4000
1/8000
1/12000</td><td colspan="4">2.5 mV (10 V)
1.25 mV (10 V)
0.83 mV (10 V)</td><td colspan="3">5 μA (20 mA)
2.5 μA (20 mA)
1.7 μA (20 mA)</td></tr>
<tr><td colspan="2">Overall accuracy</td><td colspan="7">±1.0 % (Accuracy to the maximum value)</td></tr>
<tr><td colspan="2">Maximum conversion time</td><td colspan="7">Maximum 25 msec/2 channels (same for 1 channel)</td></tr>
<tr><td colspan="2">Absolute maximum output</td><td colspan="7">Voltage: ±12 V
Current: 28 mA</td></tr>
<tr><td colspan="2">Output short circuit protection</td><td colspan="7">Provided</td></tr>
<tr><td colspan="2">Analog output points</td><td colspan="7">2 channels/module</td></tr>
<tr><td colspan="2">Insulation method</td><td colspan="7">Photocoupler insulation between output terminals and PC power
(Non-insulation between channels)</td></tr>
<tr><td colspan="2">Number of I/O points</td><td colspan="7">32 points</td></tr>
<tr><td colspan="2">Connection terminal</td><td colspan="7">20-point terminal block</td></tr>
<tr><td colspan="2">Offset/gain adjustment</td><td colspan="7">By the test switch (Without using offset/gain adjusting knobs)</td></tr>
<tr><td colspan="2">Applicable wire size</td><td colspan="7">0.75 to 1.5 mm^2</td></tr>
<tr><td colspan="2">Applicable solderless terminal</td><td colspan="7">1.25-3, 1.25- YS3A, V1.25-3, V1.25-YS3A</td></tr>
<tr><td colspan="2">Internal current consumption (5 VDC)</td><td colspan="7">0.8 A</td></tr>
<tr><td colspan="2">External dimensions mm (in.)</td><td colspan="7">130 (5.12) (H) x 34.5 (1.36) (W) x 93.6 (3.69) (D)</td></tr>
<tr><td colspan="2">Weight kg (lb)</td><td colspan="7">0.32 (0.70)</td></tr>
</table>

*1....When the offset value is set to 0 V and the gain value is set to 10 V.
*2....When the offset value is set to 4 mA and the gain value is set to 20 mA.

3.13 Wiring Instructions

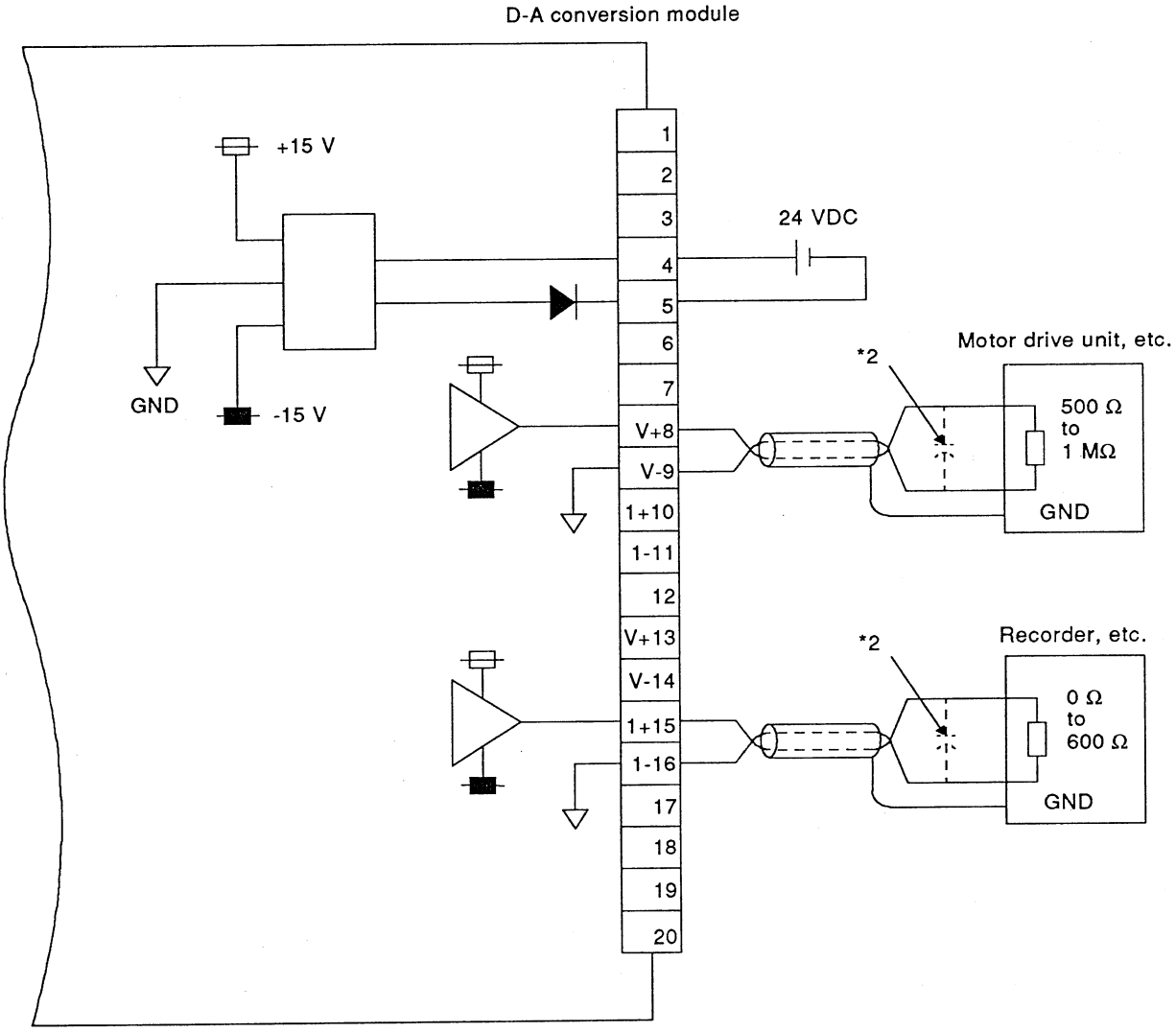
Protect external wiring against noise with the following precautions:

(1) Separate AC and DC wiring.

(2) Separate main circuit and/or high voltage wiring from control and signal wiring.

(3) Where applicable, ground the shielding of all wires to a common ground point.

3.14 Module Connection Example



*1: Use two core, shielded wiring (twisted).
*2: If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF25WV capacitor to the input terminal of external equipment.

IMPORTANT

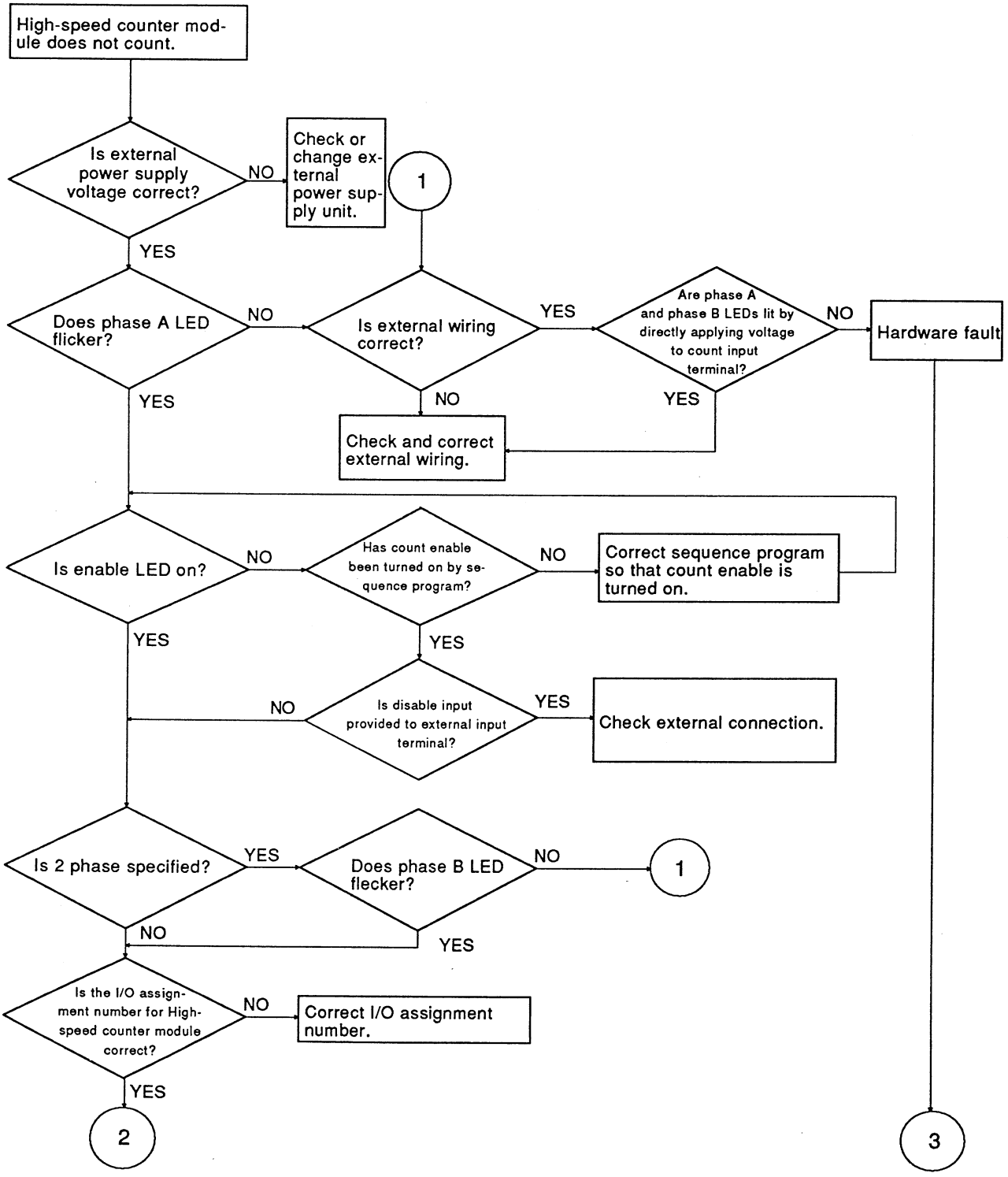
A given channel cannot be used for voltage and current outputs at the same time. Otherwise the internal elements will be damaged. Only use one set of terminals on each channel.

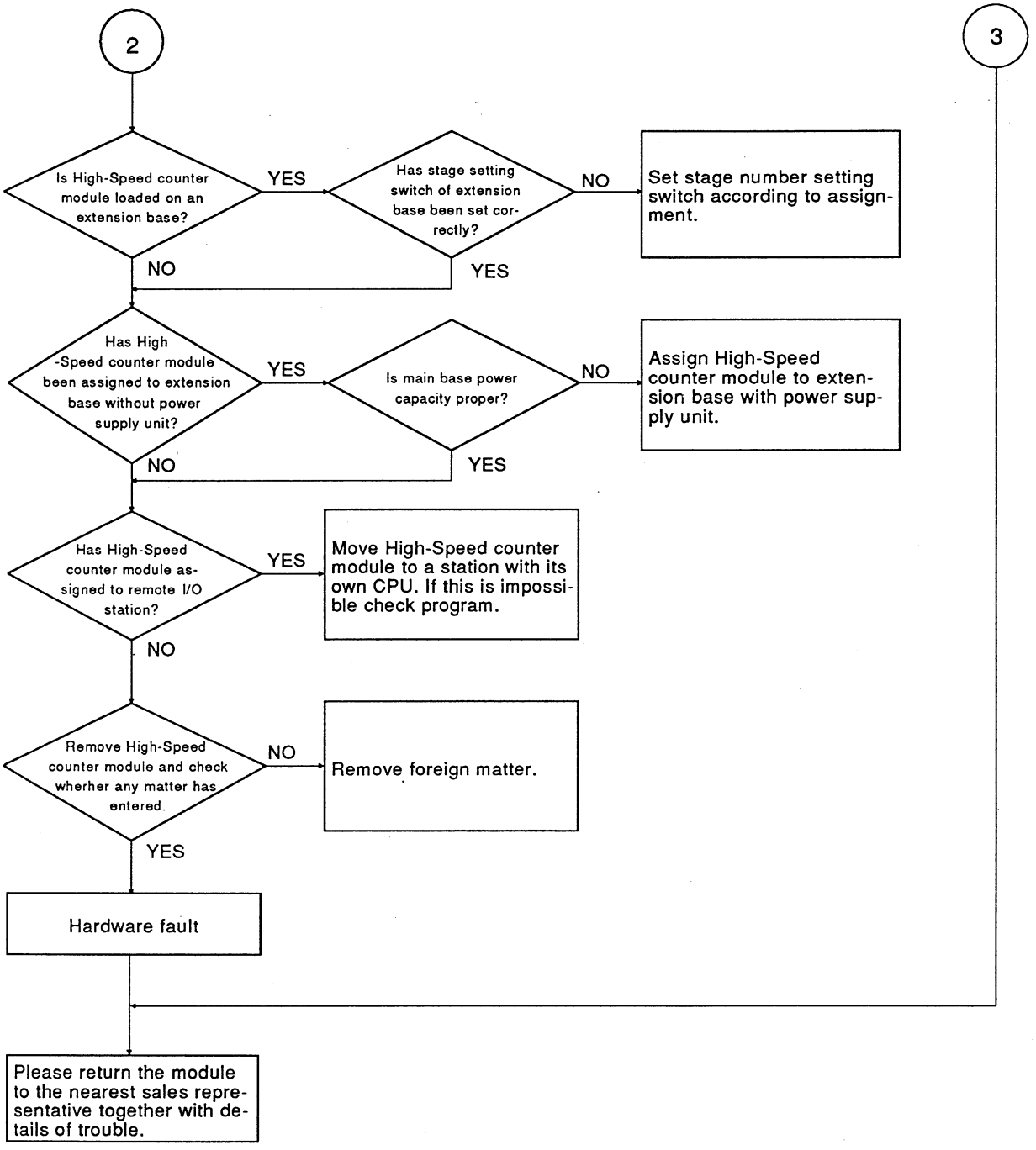
4. HIGH-SPEED COUNTER MODULES

This section explains the error descriptions and trouble shooting which can occur when high-speed counter modules are used.

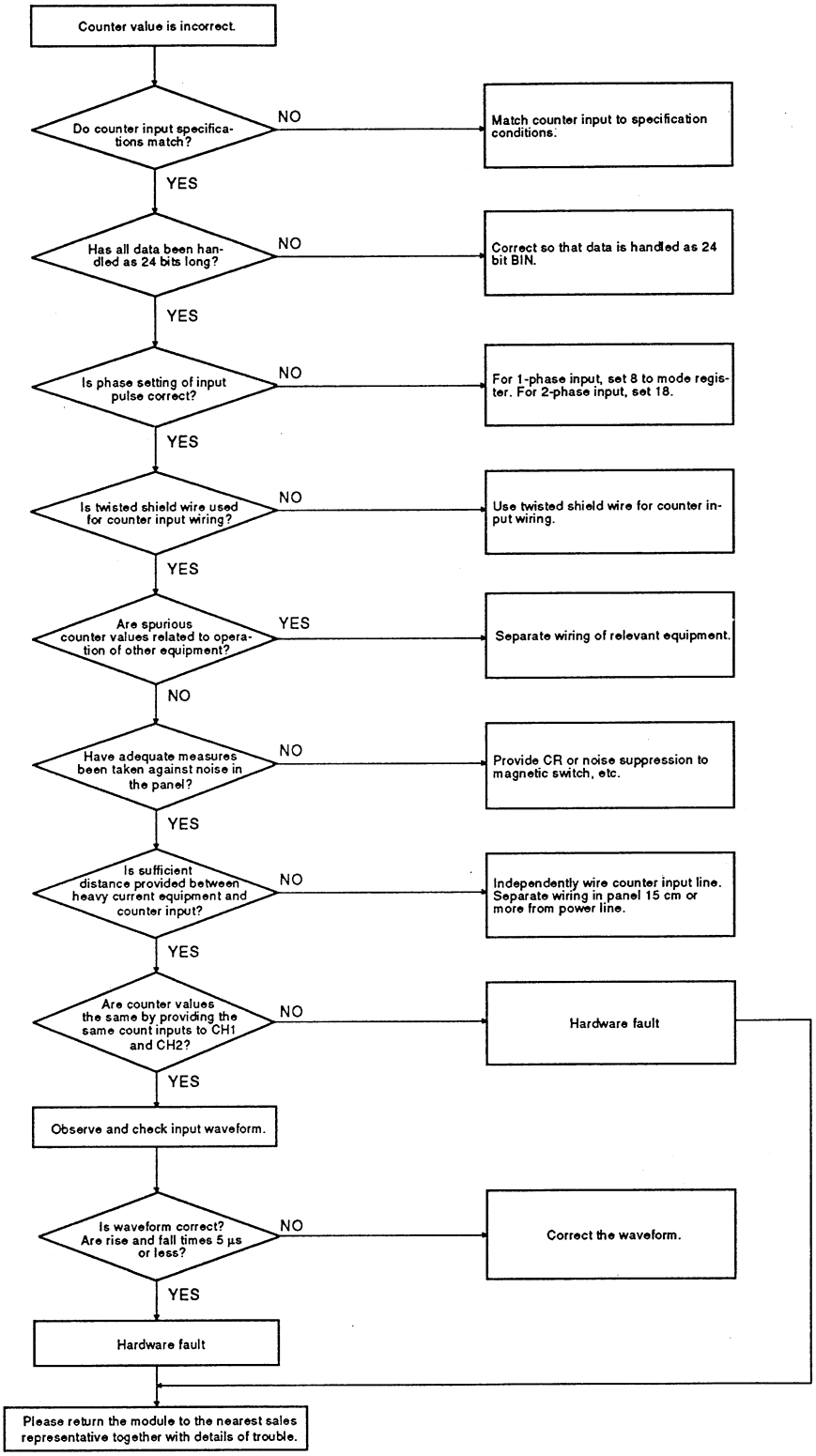
4.1 A0J2-D61, AD61, and AD61-S1 High-Speed Couter Modules

4.1.1 High-speed counter module does not count




2
3
Is High-Speed counter module loaded on an extension base?
YES
Has stage setting switch of extension base been set correctly?
NO
Set stage number setting switch according to assignment.
NO
YES
Has High -Speed counter module been assigned to extension base without power supply unit?
YES
Is main base power capacity proper?
NO
Assign High-Speed counter module to extension base with power supply unit.
NO
YES
Has High-Speed counter module assigned to remote I/O station?
YES
Move High-Speed counter module to a station with its own CPU. If this is impossible check program.
NO
Remove High-Speed counter module and check wherher any matter has entered.
NO
Remove foreign matter.
YES
Hardware fault
Please return the module to the nearest sales representative together with details of trouble.

4.1.2 Counter value is incorrect



4.2 AD61C High-Speed Counter Unit

4.2.1 Error code list

(1) If an error occurs (RUN LED blinking) when executing FROM/TO instruction, the following error codes will be stored to buffer memory address 18. Correcr as follows.

Error Code	Error and Cause	Corrective Action
100	(Read error) 1. When the FROM instruction is executed, head address number of buffer memory address is address 19 or larger. 2. An attempt is made to read words from the area exeeeding address 19. 3. An attempt is made to read write only buffer memory.	Confirm the sequence program and correct.
101	(Write error) 1. When the TO instruction is executed, head address number of buffer memory address is address 19 or larger. 2. An attempt is made to write words to the area exeeeding address 19. 3. An attempt is made to write to read only buffer memory.	Confirm the sequence program and correct.
102	Commands other than read/write have been received. Data has been rewritten due to noise.	Execute communication again. Take proper measures against noises.
103	Number of read/write specified words 0 has been received.	Execute communication again. Take proper measures against noises.
104	Data has been received when the FROM instruction is executed.	Execute communication again. Take proper measures against noises.
105	The number of words written and the number of words received are different when the TO instruction is executed.	Execute communication again. Take proper measures against noises.
1[ ]0	Values other than 8 or 18 have been written to the mode register (addresses 0 and 7). [[ ] indicates the error-generating channel number.]	Confirm the sequence program and correct. (18 will be set as the default value.)

(a) When multiple errors occur, the AD61C stores the data error code of the first error detected by the AD61C and does not store subsequent errors.

(b) The error code is reset by writing 0 to buffer memory address 18. (Written values other than 0 are ignored.)

(c) When an error occurs, if error reset is executed without restoring the error, the AD61C restores normal state, the error code becomes 0, and the RUN LED is lit stopping blinking.

POINTS

(1) When an AD61C error occurs, the A2CCPU stores a dedicated error code to special D.
(2) When an AD61C error occurs, the AJ71PT32-S3 stores the faulty station and AD61C error code to the buffer memory.

4.2.2 RUN LED is flickering/OFF

(1) When flickering

Check Item	Corrective Action
Is there data which cannot be written to or read from the AD61C?	Read the AD61C error code, confirm using the error code list in Section 4.2.1, and correct the sequence program.

(2) When OFF

Check Item	Corrective Action
Is the 24 VDC power supply charged?	• Turn On the power supply.
Is the 24 VDC within the rated voltage?	• Set the voltage to 15.6 to 31.2 V.
Is the wiring correct?	• Check for cut wires and erroneous wiring and correct.
Is there a hardware error detected (watchdog timer error)?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is OFF, AD61C hardware is faulty. Consult Mitsubishi representative.

4.2.3 LINK RUN LED is OFF

Check Item	Corrective Action
Is the RUN LED lit?	• When the RUN LED is flickering or OFF, correct according to Section 4.2.2.
Is a hardware error detected?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is off, AD61C link hardware is faulty. Consult Mitsubishi representative.

4.2.4 LINK ERR. LED is ON

Check Item	Corrective Action
Is the communication cable wiring correct?	• Confirm whether link data communication is disabled due to cable wire breakage, terminal block faulty connections or wiring faults, and correct. • If the LED does not turn off when the wiring is correct, AD61C link hardware is faulty. Consult Mitsubishi representative.

4.2.5 Count operations do not execute

Check Item	Corrective Action
Are the RUN and LINK RUN LEDs lit?	• Correct according Sections 4.2.2 and 4.2.3 if they are flickering or OFF.
Is the LINK ERR. LED OFF?	• Correct according to Section 4.2.4 is the LINK ERR. LED is ON.
Is the external wiring of phases ϕA and B correct?	• Check the external wiring and correct.
Are phases ϕA and ϕB LEDs lit by directly applying voltage to the count input terminal?	• If yes, check the external wiring and pulse generator and correct. • If no, AD61C hardware is faulty. Consult Mitsubishi representative.
Is the enable LED ON?	• If it is OFF, correct the sequence program so that it is turned ON. (Turn OFF the disable input at external input terminal.)
Do the set AD61C station number and the station number specified by the sequence program coincidence?	• With the A2CCPU, coincidence the AD61C station number and program setting. • With the AJ71PT32-S3, coincidence the program setting to the AJ71PT32-S3 buffer memory corresponding to the AD61C station number.
Is the phase specified to the AD61C buffer memory by the sequence program written with a correct value?	• Set the 1-phase specification of phase ϕA to the mode register or correct.
Are the PC CPU or AJ71PT32-S3 indicating an error?	• If it is the PC CPU, refer to the troubleshooting section of the manual of the PC CPU being used to recover correct operations. • If it is the AJ71PT32-S3, return to normal operating state according to the troubleshooting section of the AJ71PT32-S3 manual.

(1) If counter operations cannot be executed even when the above check items are correct, AD61C hardware is faulty. Consult Mitsubishi representative.

4.2.6 Count value is incorrect

Check Item	Corrective Action
Is the counter input specification correct?	• Coincidence the counter input to the specification conditions.
Are the sequence program data handled in 24-bit binary?	• Correct the sequence program so that its data can be handled in 24-bit binary.
Is the phase setting for the sequence program input pulses correct?	• For 1-phase inputs, set 8 to the mode register and for 2-phase inputs, set 18. (The default value is 18 for 2-phase inputs)
Is twisted shield wire used for counter input wiring?	• Use twised shield wire for counter input wiring.
Are spurious counter values related to the operation of other equipment?	• Separate wiring of related equipment.
Does noise come in through the ground of the AD61C?	• Disconnect the AD61C from the ground. • If the case of the AD61C contacts the ground, separate it from the ground.
Have adequate measures been taken against noise in the panel?	• Provide CR surge suppression to magnetic switches, etc.
Is sufficient distance provided between heavy current equipment and counter input line?	• Independently wire counter input line. Separate wire in panel 150 mm (5.91 in.) or more from power line.
Are counter values the same by providing the same count inputs to CH1 and CH2?	• If not, AD61C hardware is faulty. Consult Mitsubishi representative.
If the counter values are the same by providing the same count inputs to CH1 and CH2, do the pulse input waveform, rise, and fall conform to the specifications?	• Monitor and confirm the input waveform using a synchroscope. If the rise and fall are outside the specified value, resulting in a faulty waveform, correct the waveform.

(1) If counter operations cannot be executed correctly even when the above check items are correct, AD61C hardware is faulty. Consult Mitsubishi representative.

4.3 AD62C High-Speed Counter Unit

4.3.1 Error code list

(1) If an error occurs (RUN LED flashes) when executing a FROM/TO instruction, the error codes shown in Table below will be stored to buffer memory (address 12) for communications error code storage, or to (address 13) for multiple-dog setting error storage.

Error	Error Code	Cause	Corrective Action
Communication errors	100	Data has been read from buffer memory address 150 or later.	Correct the sequence program from which address 150 or later has been read.
	101	Data has been written to buffer memory addresses 0 to 4, or 150 or later.	Correct the sequence program from which addresses 0 to 4, or 150 or later have been read.
	*1 102	A command other than read (01H) or write (02H) has been received.	Take appropriate measures to prevent noise interference. Execute communications again.
	*1 103	"0" number of read/write specified words has been received.	
	*1 104	Data has been received when a FROM instruction is executed.	
	*1 105	The number of words specified for write command data is different of that of received data.	
	110	A value outside the range of 0 to 4 was set to the pulse input mode setting buffer memory (address 5)	Set a value from 0 to 4.
	111	A value outside the range of 0 to 4 was set to the counter setting buffer memory (address 6).	Set a value from 0 to 4.
	112	"0" was set to the sampling/periodic time setting buffer memory (address 11).	Set a value within the range of 1 to 65535.
	113	The preset value is the same as the ring counter value.	Set the values so that they are not the same.
	114	A preset value or counter value was written do the buffer memory while the ring counter command (Y1B) was ON.	Turn OFF the ring counter command, cancel the ring counter function, and execute the write.
Multiple-dog setting error	2( )[ ]	The ON/OFF position data setting values of dogs 0 to 3 for a channel are not in ascending order.	Set the limit switch output ON/OFF position data so that the values are in ascending order for each dog.
	3( )[ ]	A value outside the range of 0 to 4 was set in the multiple-dog setting.	Set a value of 0 to 4.

*1: These errors occur because of noise. Therefore, attempt the same operation again, and/or take appropriate measures to prevent noise interference.

( ) indicates a channel containing the first error during an operation.

[ ] indicates a dog containing the first error during an operation.

(2) The error codes for communication errors and multiple-dog setting errors are reset as shown below.

Error	Reset Operation
Communication errors	• Switch ON the communications error detection reset signal (Y04). • Write "0" to buffer memory address 12.
Multiple-dog setting errors	• Switch ON the multiple-dog setting error detection reset signal (Y1F). • Write "0" to buffer memory address 13.

4.3.2 RUN LED is flashing/OFF

(1) When flashing

Check Item	Corrective Action
Is there data which cannot be written to or read from the AD62C?	Read the AD62C error code, confirm using the error code list in Section 4.3.1, and correct the sequence program.

(2) When OFF

Check Item	Corrective Action
Is the 24 VDC power supply charged?	• Turn ON the power supply.
Is the 24 VDC within the rated voltage?	• Set the voltage to 15.6 to 31.2 V.
Is the wiring correct?	• Check for cut wires and erroneous wiring and correct.
Is there a hardware fault detected (watchdog timer error)?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is OFF, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative.

4.3.3 LINK RUN LED is OFF

Check Item	Corrective Action
Is the RUN LED lit?	• When the RUN LED is flashing or OFF, correct according to Section 4.3.2.
Is a hardware error detected?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is OFF, AD62C link hardware is faulty. Consult your nearest Mitsubishi representative.

4.3.4 LINK ERR. LED is ON

Check Item	Corrective Action
Is the communication cable wiring correct?	• Confirm whether link data communication is disabled due to cable wire breakage, terminal block faulty connections, or wiring faults, and correct. • If the LED does not turn OFF when the wiring is correct, AD62C link hardware is faulty. Consult your nearest Mitsubishi representative.

4.3.5 Count value is incorrect

Check Item	Corrective Action
Is the counter input specification correct?	• Check the counter input with the specification conditions.
Is the sequence program data handled in 32-bit binary?	• Correct the sequence program so that its data can be handled in 32-bit binary.
Is the phase setting for the sequence program input pulses correct?	• Set 0 to 4 to the mode register. (The default value is 0.)
Is twisted shield wire used for counter input wiring?	• Use twisted shield wire for counter input wiring.
Are spurious counter values related to the operation of other equipment?	• Separate wiring of related equipment.
Does noise come in through the ground of the AD62C?	• Disconnect the AD62C from the ground. • If the AD62C contacts the ground, separate it from the ground.
Have adequate measures been taken against noise in the panel?	• Provide CR surge suppression to magnetic switches, etc.
Is sufficient distance provided between heavy current equipment and counter input line?	• Independently wire counter input line. Separate wire in panel 150 mm (5.91 in.) or more from power line.
Do the pulse input waveform, rise, and fall conform to the specifications?	• Monitor and confirm the input waveform using a synchroscope. If the rise and fall are outside the specified values, resulting in a faulty waveform, correct the waveform.

(1) If counter operations cannot be executed correctly even if the above check items are correct, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative.

4.4 A1SD61 High-Speed Counter Module

4.4.1 Error code list

(1) When the FROM/TO instruction is executed, if an error occurs (RUN LED flashes), the corresponding error code number will be stored to the error code storage buffer memory (address 11) as shown in table below:

Error Code	Cause	Corrective Action
10	A value outside the range of 0 to 4 was set to the pulse input mode setting buffer memory (address 4).	Set a value from 0 to 4.
11	A value outside the range of 0 to 4 was set to the counter setting buffer memory (address 5).	Set a value from 0 to 4.
12	"0" was set to the sampling/periodic time setting buffer memory (address 10).	Set a value within the range of 1 to 65535.
13	The preset value is the same as the ring counter value.	Set the values so that they are not the same.
14	A preset value or counter value was written do the buffer memory while the ring counter command (Y13) was ON.	Turn OFF the ring counter command, cancel the ring counter function, and execute the write.
102	A write operation was attempted to addresses 0 to 3.	Delete the sequence program containing that operation.
1( )[ ]	The ON/OFF position data setting values of dogs 0 to 3 for a channel are not in ascending order.	Set the limit switch output ON/OFF position data so that the values are in ascending order for each dog.
20[ ]	A value outside the range of 0 to 4 was set in the multi-dog setting.	Set a value of 0 to 4.

* The error code is expressed as a decimal number.

( ) indicates a channel containing the first error during an operation.

[ ] indicates a dog containing the first error during an operation.

(2) When several errors occur during a single operation, only the code number of the first error detected by the A1SD61 is stored.

(3) Reset the error either by turning ON the error reset command (Y17) or by writing "0" to the data error code storage buffer memory (address 11).

After resetting the error, the RUN LED will stay lit instead of flashing.

4.4.2 RUN LED flashes or OFF

(1) When the RUN LED flashes:

Check Item	Corrective Action
Does the A1SD61 contain data that cannot be written or read?	Read the error code stored in the A1SD61 buffer memory, and take measures according to the error code.

(2) When the RUN LED is OFF:

Check Item	Corrective Action
Was a fault in the hardware (watchdog timer error) detected?	• Check to make sure the power is correctly supplied. Try turning the power supply ON and OFF several times. (Also, check if noise influences the hardware.) • When the LED remains OFF after executing the above operation, the A1SD61 may be faulty.

4.4.3 Counter value is incorrect

Check Item	Corrective Action
Is the pulse input mode consistent with the pulse input setting in the buffer memory?	Input pulses consistently with the setting.
Is the sequence program data processed as 32-bit BIN data?	Correct the sequence program so that the data is processed as 32-bit BIN data.
Is a twisted pair wire used as the pulse input wire?	Use a twisted pair wire.
Does noise come in through the ground of the A1SD61?	• Disconnect the A1SD61 from the ground. • If the A1SD61 comes in contact with the ground, separate it from the ground.
Have adequate measures been taken against noise in the panel or noise resulting from the other equipment?	Provide CR surge suppression to magnetic switches, etc.
Is sufficient distance provided between heavy current equipment and counter input line?	Wire the pulse input line independently, and separate wire in panel 150 mm (5.91 in.) or more from power line.
Do the pulses input waveform to the specifications?	Monitor and confirm the input waveform using a synchroscope. If the waveform is not consistent with the specifications, correct the waveform.

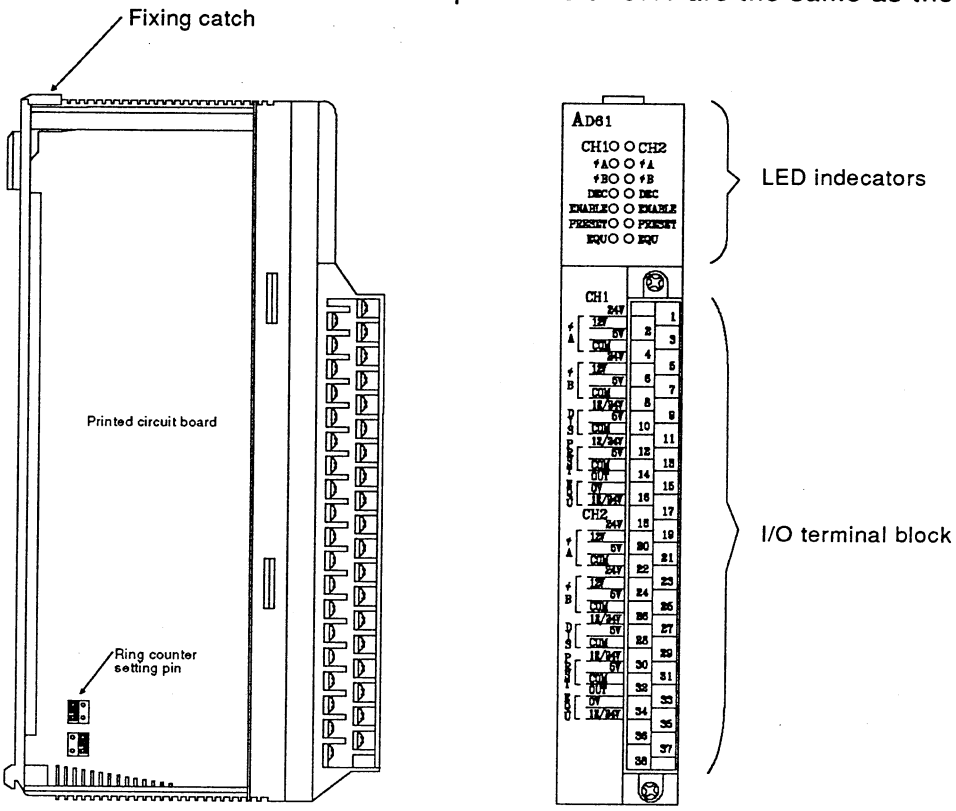
4.4.4 Count cannot be made

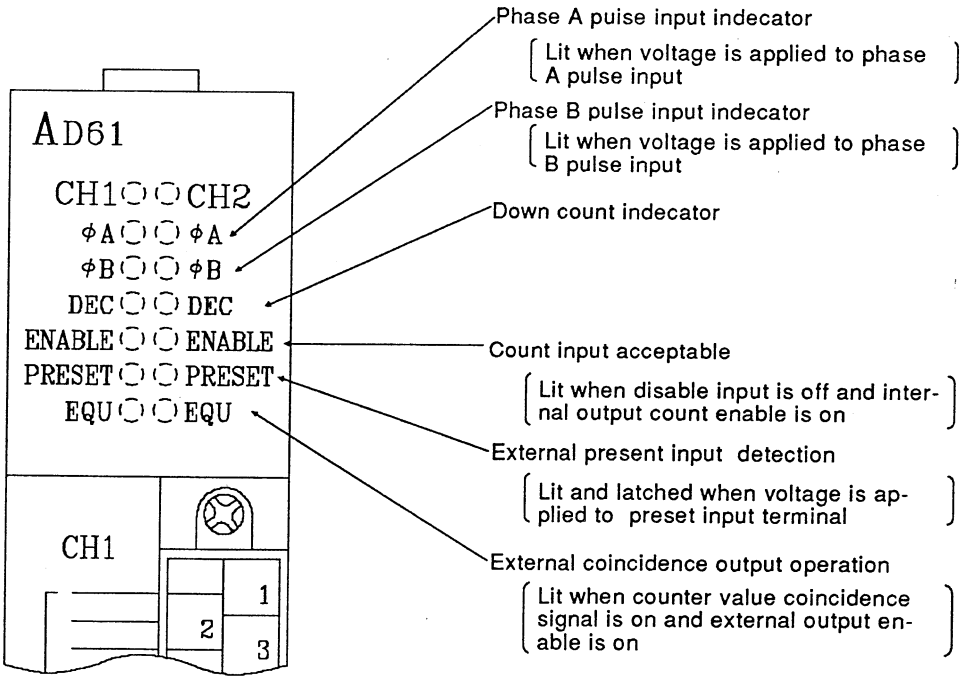
Check Item	Corrective Action
Is the external wiring of øA and øB correct?	Check the external wiring, and correct it.
When voltage is applied to the pulse input terminals øA and øB, do the LEDs of øA and øB go ON?	• When the LEDs went ON, check the external wiring and the pulse generator, and take appropriate measures. • When the LEDs did not go ON, the hardware may be faulty. In this case, consult your nearest Mitsubishi representative.
Is the count enable command (Y10) ON?	Turn ON the count enable command (Y10) with the sequence program.
Does the PC CPU signal that an error occurred?	When the PC CPU contains an error, see the troubleshooting section in the PC CPU manual, and verify the correct operation functions.
Is the counter function selection start command (Y14) ON; or is the voltage applied to the F.START terminal?	When the count disable function was set by the counter function selection, turn OFF Y14 or the F.START terminal.

4.5 Nomenclature

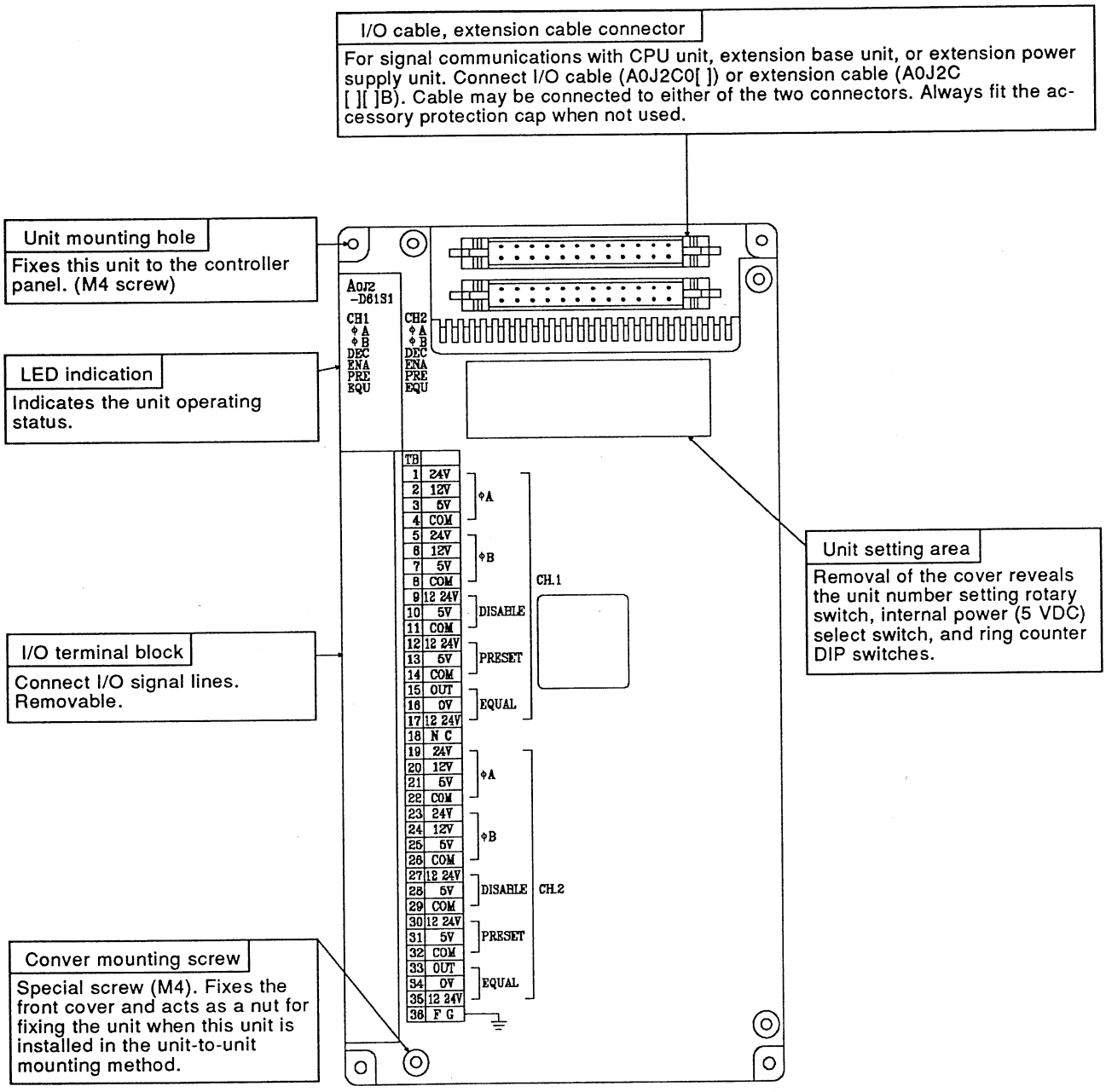
4.5.1 AD61(S1)

- LED indicators: LED "on" conditions are explained below.
  LED operations of CH1 are the same as those of CH2.

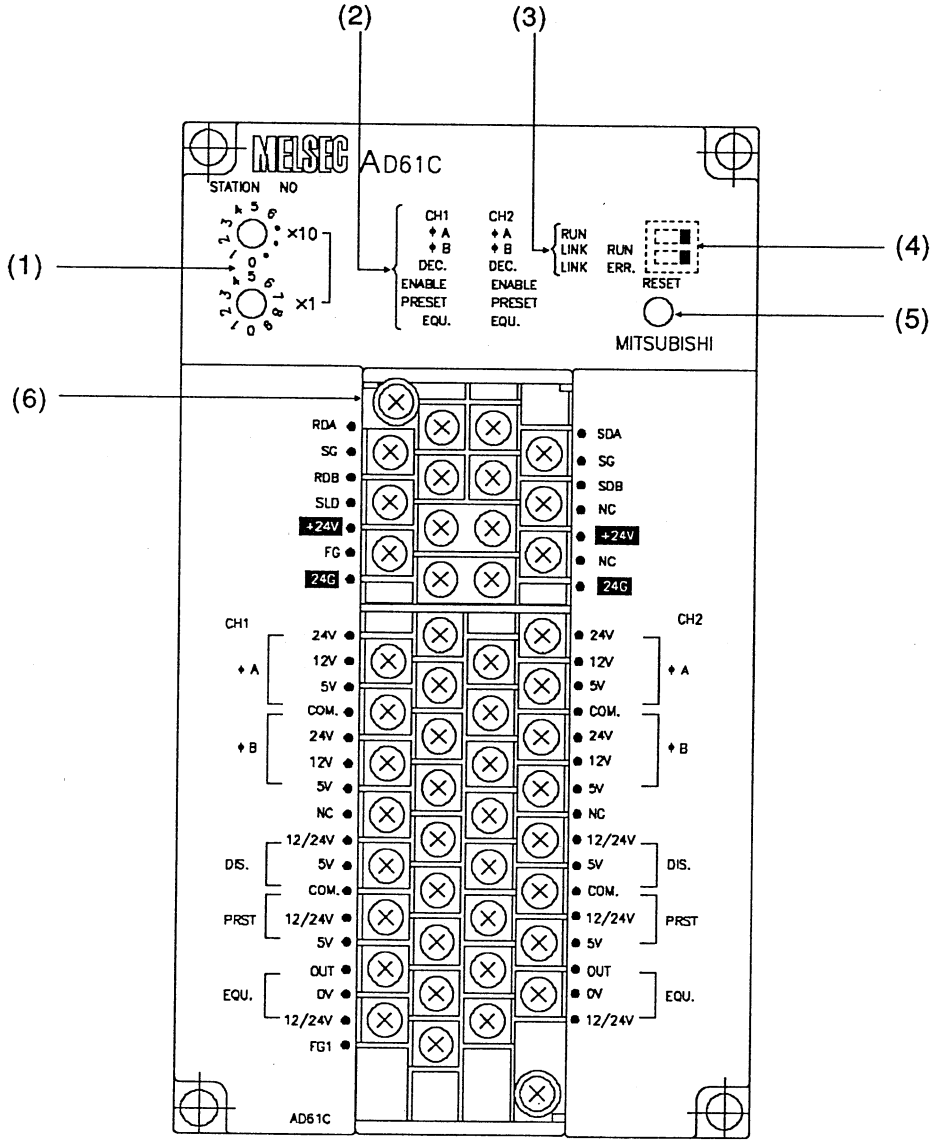




4.5.2 A0J2-D61(S1)

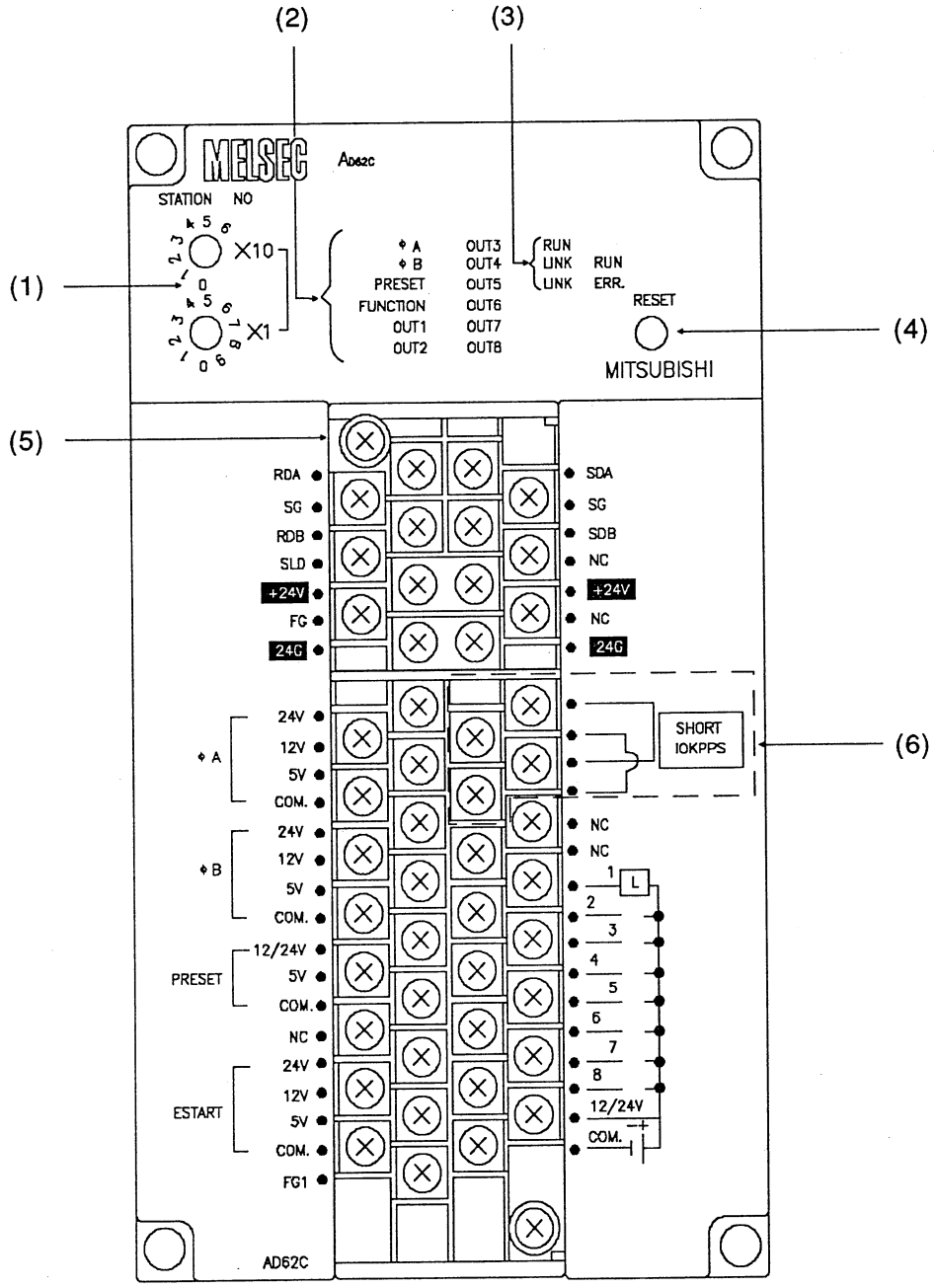


4.5.3 AD61C


(1)
(2)
(3)
(4)
(5)
(6)
MELSEC AD61C
STATION NO
×10
×1
CH1
CH2
♦A
♦B
DEC.
ENABLE
PRESET
EQU.
RUN
LINK
LINK
RUN
ERR.
RESET
MITSUBISHI
RDA
SG
RDB
SLD
+24V
FG
24G
SDA
SG
SDB
NC
+24V
NC
24G
CH1
CH2
24V
12V
5V
COM.
12/24V
OUT
0V
FG1
DIS.
PRST
EQU.
AD61C

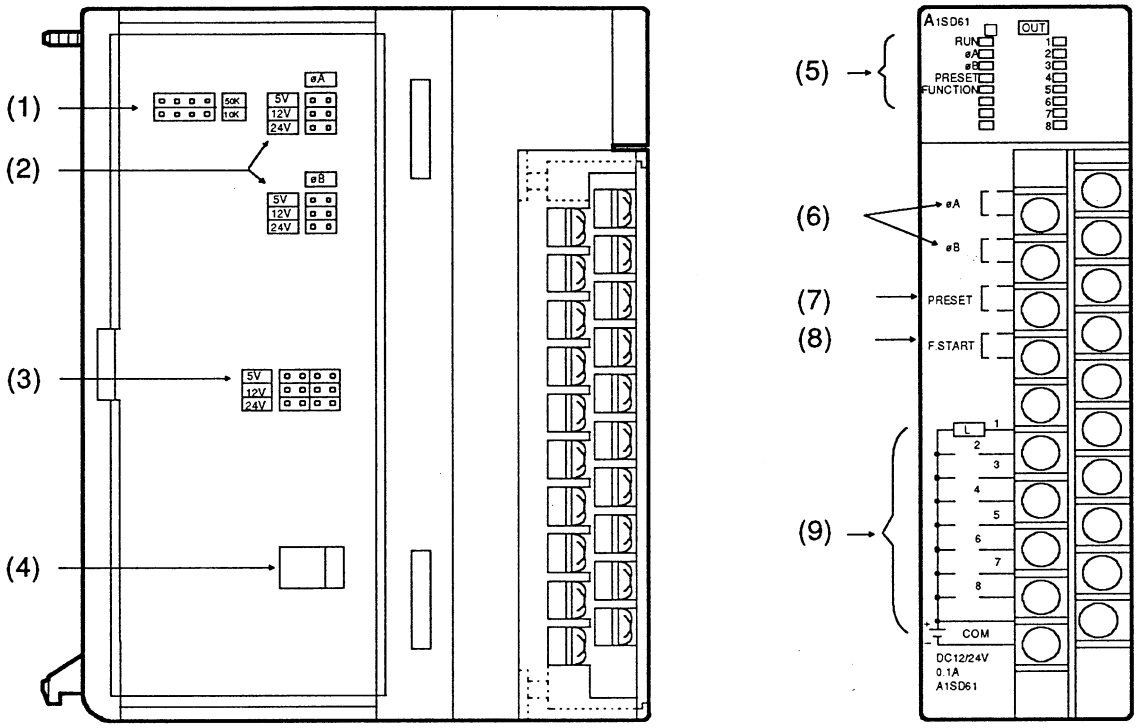
<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>(1)</td><td>Station number setting switch</td><td>• Sets the station number from 01 to 61 by rotary switch.
• Station 00 is a bypass function.</td></tr>
<tr><td>(2)</td><td>CH1, CH2 operating status indication LED</td><td>LEDs for operating status indication
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>ϕ A (phase A pulse input indication)</td><td>Lit when voltage is applied to phase A pulse input terminal</td></tr>
<tr><td>ϕ B (phase B pulse input indication)</td><td>Lit when voltage is applied to phase B pulse input terminal</td></tr>
<tr><td>DEC (operation in progress indication)</td><td>• Lit at 1-phase decrement specification
• Lit at 2-phase decrement specification</td></tr>
<tr><td>ENABLE (count input enable)</td><td>• Lit when disable input is OFF and count enable is ON</td></tr>
<tr><td>PRESET (external preset input detection)</td><td>• Lit and latched when voltage is applied to preset input terminal
• OFF when external preset detection reset signal is ON</td></tr>
<tr><td>EQU (external coincidence output operation in progress)</td><td>• Lit when the counter value coincidence signal and the external output enable are ON</td></tr>
</table></td></tr>
<tr><td>(3)</td><td>Operation state indicator LED</td><td>LEDs for operating status, and error definition indecation, etc.
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>RUN</td><td>• ON: Normally running
• Flicker: Write data error
• OFF: 24 VDC is off or WDT error</td></tr>
<tr><td>LINK RUN</td><td>• ON: Link is normal
• OFF: Link error is detected at power on.</td></tr>
<tr><td>LINK ERR.</td><td>• ON: Error is detected during link.
• OFF: Link is normal</td></tr>
</table></td></tr>
<tr><td>(4)</td><td>Ring counter setting switch</td><td>Switch for setting ring counter function</td></tr>
<tr><td>(5)</td><td>Reset switch</td><td>AD61C hardware reset (initialization) switch</td></tr>
<tr><td>(6)</td><td>I/O terminal block</td><td>• Terminal block for data link cable wiring, 24 V power supply wiring, CH1, CH2 I/O wiring.</td></tr>
</table>

4.5.4 AD62C


(1)
(2)
(3)
(4)
(5)
(6)
MELSEC
AD62C
STATION NO
X10
X1
PRESET
FUNCTION
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
RUN
LINK
LINK
RUN
ERR.
RESET
MITSUBISHI
RDA
SG
RDB
SLD
+24V
FG
24G
SDA
SG
SDB
NC
+24V
NC
24G
SHORT
IOKPPS
24V
12V
5V
COM.
12/24V
NC
ESTART
FG1
L
12/24V
COM.
AD62C

<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>(1)</td><td>Station number setting switches</td><td>• Sets the station number from 01 to 61 using rotary switches.
• Station 00 is a bypass function.</td></tr>
<tr><td>(2)</td><td>Operating state indicator LEDs</td><td>Operating state indicator LEDs
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>øA (A input indicator)</td><td>Lit when voltage is applied to the phase A pulse input terminal.</td></tr>
<tr><td>øB (B input indicator)</td><td>Lit when voltage is applied to the phase B pulse input terminal.</td></tr>
<tr><td>PRESET (external preset input detection)</td><td>• Lit and latched when voltage is applied to the preset input terminal.
• OFF when the external preset detection reset signal is ON.</td></tr>
<tr><td>FUNCTION</td><td>Lit when voltage is applied to the F.START terminal.</td></tr>
<tr><td>OUT 1 to OUT 8</td><td>Limit switch output function. Lit by turning ON the limit switches of each channel. Turned OFF by turning OFF the limit switches of each channel.</td></tr>
</table></td></tr>
<tr><td>(3)</td><td>Operating state indicator LEDs</td><td>Operating state, error contents, etc. indicator LEDs
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>RUN</td><td>• ON ..... Running normally
• Flashing .... Write data error
• OFF ..... 24 VDC is OFF or a WDT error</td></tr>
<tr><td>LINK RUN</td><td>• ON ..... Link is normal.
• OFF ..... Link error detected during power ON.</td></tr>
<tr><td>LINK ERR.</td><td>• ON ..... Detected.
• OFF ..... Link is normal.</td></tr>
</table></td></tr>
<tr><td>(4)</td><td>Reset switch</td><td>AD62C hardware reset (initialization) switch</td></tr>
<tr><td>(5)</td><td>I/O terminal block</td><td>• Terminal block for data link cable wiring, 24 V power supply wiring, and I/O wiring.</td></tr>
<tr><td>(6)</td><td>Count speed switching terminal</td><td>• Switches setting between 50K and 10K by shorting or opening these terminals.</td></tr>
</table>

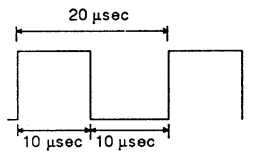
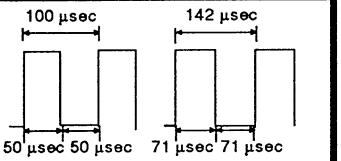
4.5.5 A1SD61



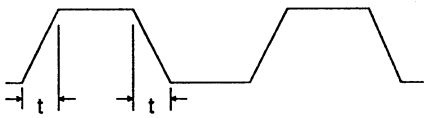
No.	Name		Description
(1)	Counting speed setting pin		50K: Counts pulses at a maximum speed of 50K pps in 1-phase or 2-phase input. 10K: Counts pulses at 10K pps in 1-phase input, at 7K pps in 2-phase input. (The factory-setting is 50K.)
(2)	Pulse input voltage setting pin		Sets the pulse voltage that is input to Phase A or B. (The factory-setting is 24 V.) Mitsubishi cannot guarantee the module when a pulse whose voltage is higher than the set voltage is applied.
(3)	External input voltage setting pin		Sets the voltage input to the PRESET/F.START terminals. (The factory-setting is 24 V.) Mitsubishi cannot guarantee the module when a pulse whose voltage is higher than the set voltage is applied.
(4)	Fuse		Used for protecting OUTs 1 to 8 from overcurrent.
(5)	LED indicators	RUN	Lit when the module operates normally. Flashes when a data write error has occurred. OFF when a watchdog timer error has occurred.
		øA	Lit when voltage is applied to phase A pulse input terminal.
		øB	Lit when voltage is applied to phase B pulse input terminal.
		PRESET	Lit and latched when voltage is applied to the PRESET terminal. OFF when external preset detection reset signal (Y16) is turned ON.
		FUNCTION	ON when voltage is applied to the F. START terminal.
		OUTs 1 to 8	ON when a corresponding limit switch is turned ON by the limit switch output function. OFF when the limit switch is turned OFF.
(6)	øA/øB		Pulse input terminals (ϕB is used as decrement count command.)
(7)	PRESET		The terminal in which voltage is applied when a preset is executed from an external device.
(8)	F.START		The terminal in which voltage is applied when a counter function selection is executed.
(9)	OUTs 1 to 8		An external output terminal used for limit switch output.

4.6 Performance Specifications

4.6.1 AD61(S1)

Item			Specifications	
			AD61	AD61S1
I/O points			32 points	
Number of channels			2 channels	
Performance specifications of 1 channel	Count input signal	Phase	1-phase input, 2-phase input	
		Signal level (Phase A, Phase B)	5 VDC 12 VDC 24 VDC } 2 to 5 mA	
	Counter	Counting speed *(Maximum)	1-phase input: 50 KPPS 2-phase input: 50 KPPS	1-phase input: 10 KPPS 2-phase input: 7 KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)	
		Form	Up/down preset counter plus ring counter function	
		Minimum count pulse width Set input rise and fall times to 5 µsec.or less. Duty ratio: 50 %	 (1-, 2-phase inputs)	 (1-phase input) (2-phase input)
	Magnitude comparison between CPU and AD61	Comparison range	24 bits, binary	
		Comparison result	Set value < count value Set value = count value Set value > count value	
	External input	Preset	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
		Count disable	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
	External output	Coincidence output	Transister (open collector) output 12/24 VDC, 0.5 A	
Current consumption			5 VDC, 0.3 A	
Weight			0.5 kg (1.1 lb)	

*: Counting speed is influenced by pulse rise time and fall time and fall time. Countable speeds are as follows. (If a pulse greater than 50 µsec. is counted by the AD61, miscounting may occur. In this case, use the AD61S1.)

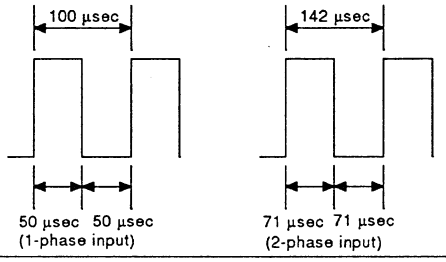


(1) AD61 (for both 1 and 2 phase inputs)
t = 5 µs----50 KPPS
t = 50 µs---5 KPPS

(2) AD61S1

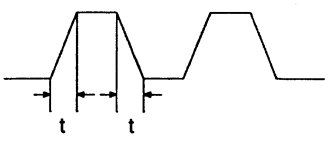
Rise/Fall Time	1 Phase Input	2 Phase Input
t = 5 µs	10 KPPS	7 KPPS
t = 500 µs	500 PPS	250 PPS

4.6.2 A0J2-D61(S1)

Item			Specifications
I/O points			64 points
Number of channels			2 channels
Performance specifications of 1 channel	Count input signal	Phase	1-phase input, 2-phase input
		Signal level (Phase A, Phase B)	5 VDC 12 VDC 24 VDC } 2 to 5 mA
	Counter	Counting speed *(Maximum)	1-phase input: 10 KPPS 2-phase input: 7 KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)
		From	Up/down preset counter plus ring counter function
		Minimum count pulse width (Set input rise and fall times to 5 µs. or less. Duty ratio: 50 %)	
	Magnitude comparison between CPU and D61S1	Comparison range	24 bits, binary
		Comparison result	Set value < count value Set value = count value Set value > count value
	External input	Preset	12/24 VDC, 3/6 mA 5 VDC, 5 mA
		Count disable	12/24 VDC, 3/6 mA 5 VDC, 5 mA
	External output	Coincidence output	Transistor (open collector) output 12/24 VDC, 0.5 A
Current consumption			5 VDC, 0.1 A
Weight kg (lb)			0.65 (1.43)

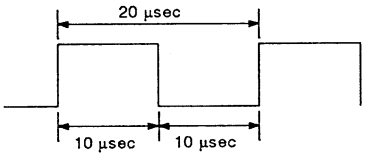
*: Counting speed is influenced by pulse rise time and fall time. Countable speeds are as follows.

Rise/Fall Time	1 Phase Input	2 Phase Input
t = 5 µs or less	10 KPPS	7 KPPS
t = 500 µs	500 PPS	250 PPS

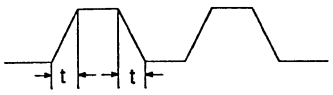


If the rise ro fall time is more than 500 µs, miscount may occur. Use the A0J2-D61(S1) at 500 µs or less.

4.6.3 AD61C

Item			Specifications	
Number of occupied stations (number of occupied points)			4 stations (32 points)	
Number of channels			2 channels	
Performance specifications of 1 channel	Count input signal	Phase	1-phase input, 2-phase input	
		Signal level (Phase A, Phase B)	5 VDC 12 VDC 24 VDC } 2 to 5 mA	
	Counter	Counting speed *(Maximum)	1-phase input	50 KPPS
			2-phase input	50 KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)	
		From	Increment/decrement preset counter plus ring counter function	
		Minimum count pulse width (1-, 2-phase inputs)	 Rise time and fall time of input should be 5 µsec or less each. Duty ratio: 50 %	
	Magnitude comparison between CPU and AD61C	Comparison range	24 bits, binary	
		Comparison result	Set value ≤ count value Set value = count value Set value > count value	
	External input	Preset	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
		Count disable	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
	External output	Coincidence output	Transistor (open collector) output 12/24 VDC, 0.3 A	
Maximum transmission distance between stations			50 (twisted pair cable 0.3 mm^2 (164.05 ft)) 100 (twisted pair cable 0.5 mm^2 (328.1 ft)) } Unlimited total distance	
24 VDC internal current consumption (A)			0.15	
External dimensions mm (in.)			170 (6.69) x 100 (3.94) x 80 (3.15)	
Weight kg (lb)			1.0 (2.2)	

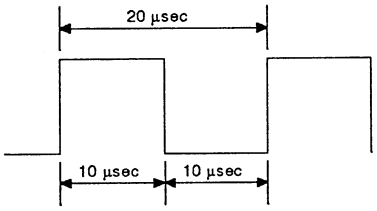
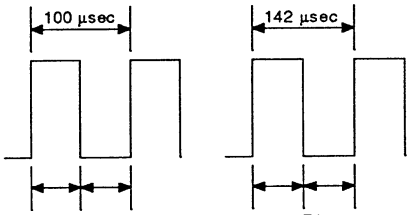
*: (1) The pulse rise/fall time determines whether the counting speed is correct or incorrect. Countable pulse inputs are as follows.



(For both 1 and 2 phase inputs)
t = 5 µs ..... 50 KPPS
t = 50 µs .... 5 KPPS

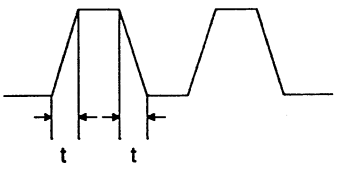
(2) If a pulse input has greater than t = 50 µsec, the AD61C may miscount and cannot be used.

4.6.4 AD62C

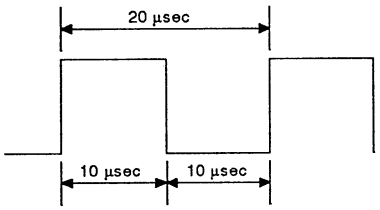
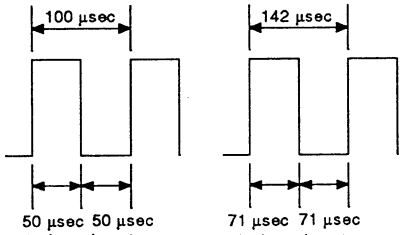
Item		Specifications		
Counting speed switching		50 KPPS		10 KPPS
Number of I/O occupied points		4 stations (32 points)		
Number of channels		1 channel		
Count input signal	Phase	1-phase and 2-phase inputs		
	Signal levels (øA and øB)	5 VDC 12 VDC 24 VDC } 2 to 5 mA		
Counter	Maximum counting speed *	1-phase input	50 KPPS	10 KPPS
		2-phase input	50 KPPS	7 KPPS
	Counting range	32-bit signed binary -2147483648 to 2147483647		
	Type	Equipped with UP/DOWN preset counter and ring counter functions		
	Minimum pulse width that can be counted (Adjust so that the leading edge/fall time of the input is 5 µsec or less. Duty ratio: 50 %)	 (1-phase input and 2-phase inputs)		 (1-phase input) (2-phase input)
Limit switch output	Comparison range	32-bit signed binary		
	Comparison result	N/O contact operation: dog ON address ≤ count value ≤ dog OFF address N/C contact operation: dog OFF address ≤ count value ≤ dog ON address		
External input	Preset	12/24 VDC 3/6mA 5 VDC 5 mA		
	Function start			
External output	Comparison output	Transistor (open collector) output 12/24 VDC 0.1 A/point 0.8 A/common		
Power consumption		24 VDC 0.15 A		
Weight (kg) (lb)		0.86 (1.91)		

* The counting speed is influenced by the pulse leading edge/fall time. The following counting speeds are possible. If a pulse is counted with a leading edge/fall time that is too long, a counter error may be caused.

Leading Edge/fall Time	Counting Speed Switching			
	50K		10K	
	1-phase Input	2-phase Input	1-phase Input	2-phase Input
t=5 µsec or less	50 KPPS	50 KPPS	10 KPPS	7 KPPS
t=50 µsec or less	5 KPPS	5 KPPS	1 KPPS	700 PPS
t=500 µsec	—	—	500 PPS	250 PPS

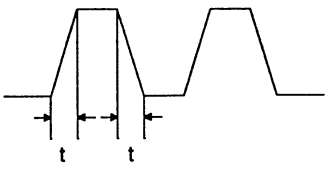


4.6.5 A1SD61

Item		Specifications		
Counting speed switching pin		50 KPPS		10 KPPS
Number of I/O occupied points		32 points		
Number of channels		1 channel		
Count input signal	Phase	1-phase and 2-phase inputs		
	Signal levels (øA and øB)	5 VDC 12 VDC 24 VDC } 2 to 5 mA		
Counter	Maximum counting speed *	1-phase input	50 KPPS	10 KPPS
		2-phase input	50 KPPS	7 KPPS
	Counting range	32-bit signed binary -2147483648 to 2147483647		
	Type	Equipped with UP/DOWN preset counter and ring counter functions		
	Minimum pulse width that can be counted (Adjust so that the leading edge/fall time of the input is 5 µsec or less. Duty ratio: 50 %)	 (1-phase and 2-phase inputs)		 50 µsec 50 µsec (1-phase input) 71 µsec 71 µsec (2-phase input)
Limit switch output	Comparison range	32-bit signed binary		
	Comparison result	N/O contact operation: dog ON address ≤ count value ≤ dog OFF address N/C contact operation: dog OFF address ≤ count value ≤ dog ON address		
External input	Preset	12/24 VDC 3/6 mA 5 VDC 5 mA		
	Function start			
External output	Comparison output	Transistor (open collector) output 12/24 VDC 0.1 A/point 0.8 A/common		
Power consumption		5 VDC 0.35 A		
Weight kg (lb)		0.27 (0.60)		

* The counting speed is influenced by the pulse leading edge/fall time. The following counting speeds are possible. If a pulse is counted with a leading edge/fall time that is too long, a counter error may be caused.

Counting Speed Setting Pin	50 K		10 K	
Leading Edge/fall Time	1-phase Input	2-phase Input	1-phase Input	2-phase Input
t=5 µsec or less	50 KPPS	50 KPPS	10 KPPS	7 KPPS
t=50 µsec or less	5 KPPS	5 KPPS	1 KPPS	700 PPS
t=500 µsec	—	—	500 PPS	250 PPS



4.7 Wiring Instructions

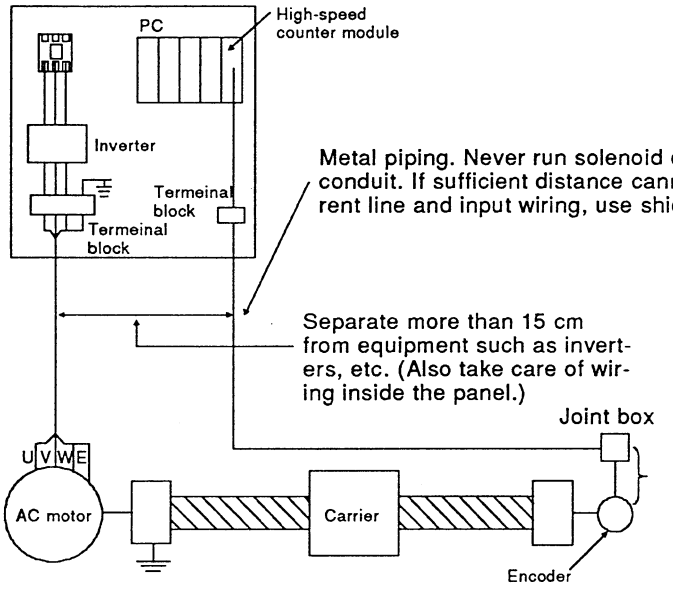
When using high speed pulse inputs take precautions against noise in all wiring.

1) Be sure to use shielded twisted pair wires. Also provide Class 3 grounding.

2) Do not run a twisted pair wire in parallel with any power line, I/O line, etc. which may gererate noise. It is necessary to run the twisted pair wire separately from the above described lines and over the shortest possible distance.

3) A stabilized power supply is necessary for the pulse generated. For 1-phase input, connect count input signal only to phase A. For 2-phase input, connect count input signal to phase A and phase B.

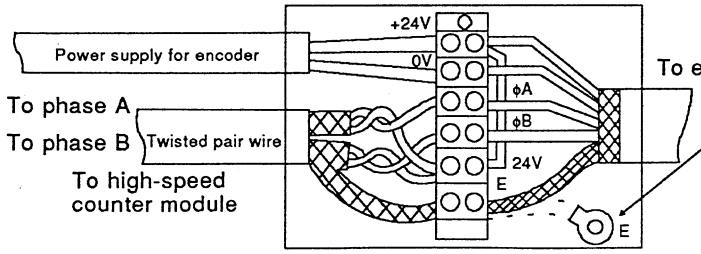
Special care must be taken to prevent the input wiring from picking up noise. The diagram below indicates the type of precautions required.



Distance between encoder and joint box should be as short as possible. If the distance from the AD61 to the encoder is too long an excessive voltage drop occurs. Therefore, measure the voltage during operation and check that she voltages are within the rated voltage of tha encoder. If the voltage drop is large, increase the size of wiring or use an encoder of 24 VDC with less current consumption.

4.8 Connection Example

- Ground twisted shield wire on the encoder side (joint box). (This is a connection example for 24 V sink load.)



Connect the encoder shield wire to the twisted pair shield wire inside the joint box. If the shield wire of the encoder is not grounded in the encoder, ground it inside the joint box as indicated by dotted line.

5. MELSECNET II

It is important to use a device with high reliability to improve the reliability of a system.
In addition, it is improtant to be able to recover from a mulfunction surely within a short period of time. This Section explains the following basic two methods to recover from a mulfunction surely and in a short time.

(1) Link monitoring using GPP, HGP and PHP

(2) Moniroring special relay (M) and special data register

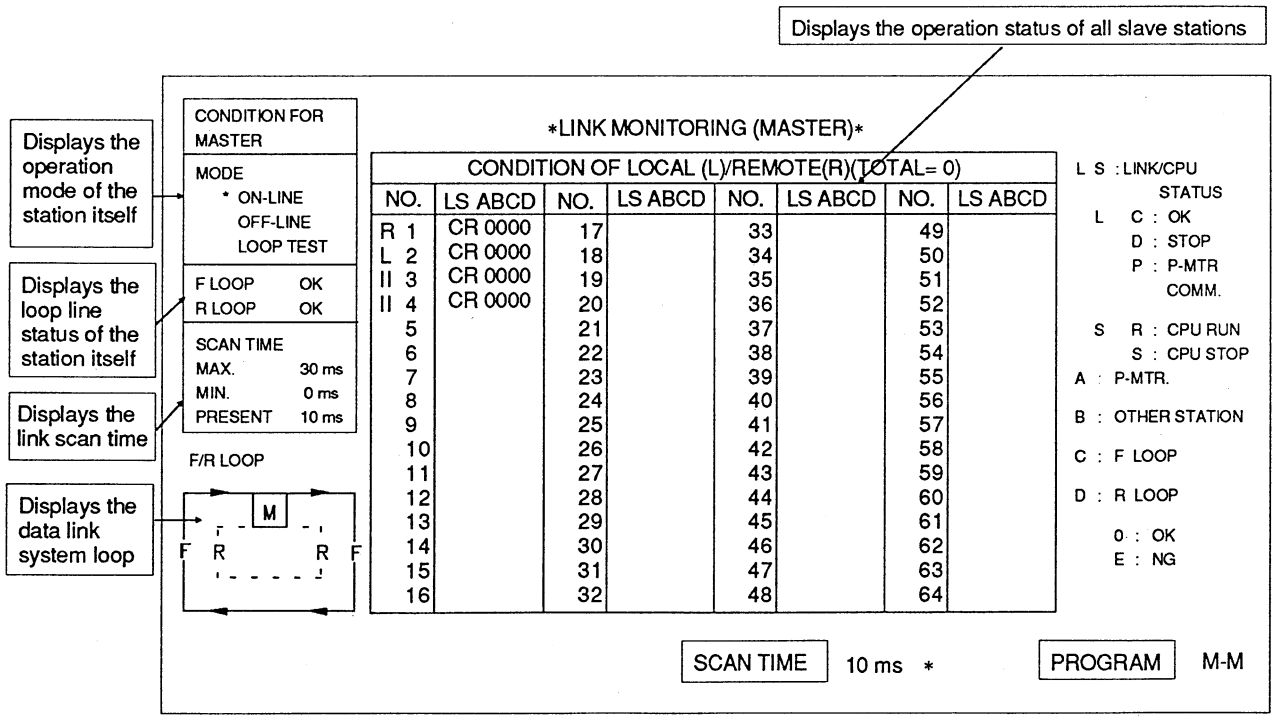
5.1 Link Monitoring by Using GPP, HGP and PHP

When link monitoring is designated by using GPP, HGP and PHP, the link state of data link system can be monitored by batch. Therefore, the loop state and the state of master station or slave station and a scan time, etc. can be monitored. The monitoring contents are the same as the contents of the link special relay and the special register. There are monitoring for a master station, for remote I/O, and for a local station. When GPP is installed in a master station , a monitor screen for a master station is used. When GPP is installed in a local station, a monitor screen for a local station is used. When GPP is installed in a remote I/O station, a monitor screen for a remote I/O station is used. Refer to the GPP operation manual about the method of operating GPP.

(1) Monitor screen for a master station

When GPP is installed in a master station, this monitor screen is used.

5.1.1 Master station link monitor



(1) Host station operation mode

(a) Displays the master station operation status

1) ONLINE:

Master station mode setting is ONLINE (automatic return function set/not set).

2) OFFLINE:

Master station mode setting is OFFLINE, SELF-LOOPBACK TEST, or STATION-TO-STATION TEST.

3) LOOP TEST:

Master station mode setting is FORWARD LOOP TEST or REVERSE LOOP TEST.

(b) The selected operation mode is stored in M9224 and M9227.

(2) Loop line status of the station itself

(a) Displays the forward loop (F loop) and reverse loop (R loop) status of the master station.

1) OK : Loop line is normal.

2) NG : Loop line is faulty.

(b) The loop line status is stored in M9225 and M9226.

(3) Link scan time

(a) Displays the required link scan time between the master station and a local station.

1) AX : Displays the maximum link scan time.

2) MIN : Displays the minimum link scan time.

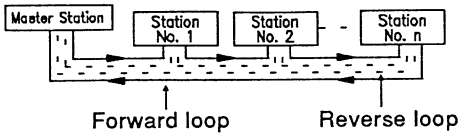
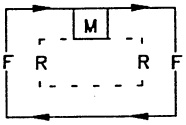
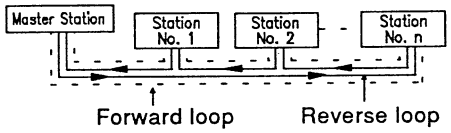
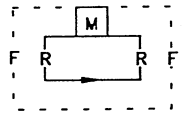
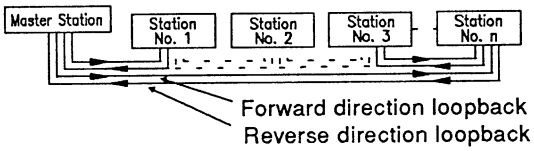
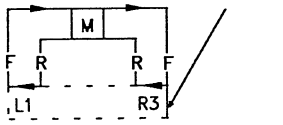
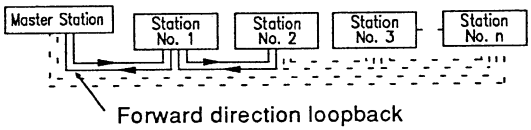
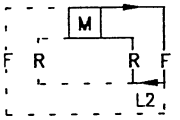
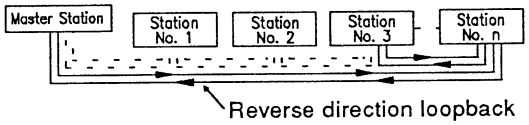
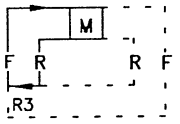
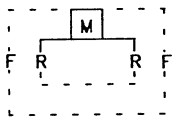
3) PRESENT : Displays the presently required link scan time.

(b) The link scan time is stored in D9207 to D9209.

(4) Data link system loop status

(a) The table on the following page illustrates how the status of loop currently being used for the link is displayed.

Data Link Status

Data Link Status	GPP/PHP Screen Display
Data link in forward loop 	
Data link in reverse loop 	
Loopback in forward/reverse direction 	Loopback station L: Local station R: Remote I/O station 
Loopback in forward direction 	
Loopback in reverse direction 	
Data link impossible	

(b) The loop line status and loopback station are stored in the following registers:

1) Loop line status : D9204

2) Loopback station : D9205, D9206

(5) Operation status of all slave stations (local and remote I/O stations)

The following describes how the status of all of the slave stations in the system is displayed:

"L" column: Status of present data link

"C": Communicating normally

"D": Disconnected due to communication stop

Possible causes for "D" being displayed:

(1) The power supply to the disconnected station is FF.

(2) The disconnected station was reset.

(3) An error occurred that caused PC CPU operations to stop.

(4) A MELSECNET-compatible local or remote I/O station has been connected to a station number that has been set with link parameters as a MELSECNET (II)-compatible station (local station).

(5) The station was disconnected as part of loopback processing.

"P": Parameter communication with master station

Link parameter communication is only executed once when starting communications.

Possible causes for "P" being displayed continuously:

(1) A remote I/O station is connected to a station number set with the link parameters as the MELSECNET mode local station.

(2) A local station is connected to a station number set as a remote I/O station.

(3) A remote I/O station is connected to a station number set as a MELSECNET-compatible local station with link parameters in the MELSECNET II composite mode.

"C" and "D" data are stored in special data registers D9224 to D9227.

(This data is the same as the data in D9224 and D9225 when a MELSECNET/B Data Link System is used.)

"P" data is stored in special data registers D9228 to D9231.

(This data is the same as the data in D9228 and D9229 when a MELSECNET/B Data Link System is used.)

"S" column: Present CPU operation status

"R" : Run status

"S" : Stop status

"R" will always be displayed for a remote I/O station.

The data displayed in the "S" column is stored in special data registers D9212 to D9215.

(This data is the same as the data in D9212 and D9213 when a MELSECNET/B Data Link System is used.)

"A" column: An error will occur with the master station for the third tier if there is an error in the third tier link parameters set for the station in question.

For example, an error will occur if neither inputs (X) nor outputs (Y) are set with the link parameters or if the I/O module is not loaded in the slots as allocated by the master station I/O allocation.

"0" : Normal

"E" : Error

The data displayed in the "A" column is stored in special data registers D9220 to D9223.

(This data is the same as the data in D9220 and D9221 when a MELSECNET/B Data Link System is used.)

"B" column: Displays whether a local station has detected an error at another local station.

"0" : Error has not been detected.

"E" : Error has been detected.

"0" will always be displayed for a remote I/O station.

The data displayed in the "B" column is stored in special data registers D9216 to D9219.

(This data is the same as the data in D9216 and D9217 when a MELSECNET/B Data Link System is used.)

"C" column: Displays the forward loop line status of each slave station.

"0" : Normal

"E" : Error

The data displayed in the "C" column is stored in special data registers D9232 to D9239.

(This data is the same as the data in D9232 to D9235 when a MELSECNET/B Data Link System is used.)

"D" column: Displays the reverse loop line status of each slave station.

"0" : Normal

"E" : Error

The data displayed in the "C" column is stored in special data registers D9232 to D9239.

(This data is the same as the data in D9232 to D9235 when a MELSECNET/B Data Link System is used.)

POINTS

(1) Forward/reverse loop errors of the master station and slave stations are detected at the receive end.

Possible causes for forward/reverse loop errors:

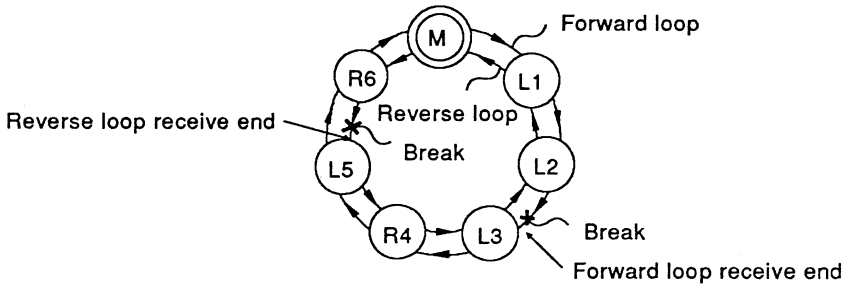
(a) Broken or loose loop cable connection

(b) Faulty hardware at receive end

(c) Faulty hardware at send end

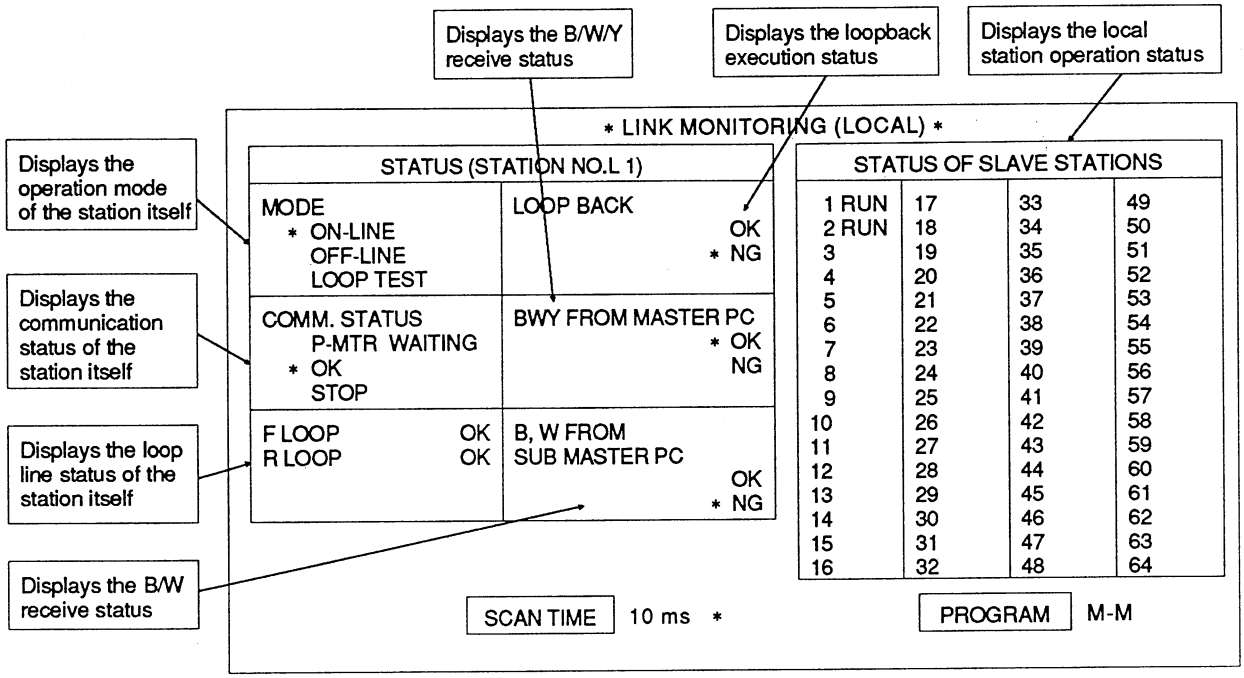
In the system configuration illustrated below, if the forward loop of L3 becomes faulty, the forward loop cable that connects L2 to L3 might be broken or loose, the hardware at the forward loop send end of L2 might be faulty, or the hardware at the forward loop receive end of L3 might be faulty.

If the cable that connects L5 and R6 is broken or loose, a reverse loop error for L5 will occur.



(2) If the status of a slave station displayed in "L" column is "D", the previous data in the "S", "A", "B", "C", and "D" columns will remain unchanged.

5.1.2 Local station link monitor



(1) Operation mode of the station itself

(a) Displays the local station operation status

1) ONLINE:

Local station mode setting is ONLINE (automatic return function set/not set).

2) OFFLINE:

Local station mode setting is OFFLINE, SELF-LOOPBACK TEST, or STATION-TO-STATION TEST.

3) LOOP TEST:

Local station mode setting is FORWARD LOOP TEST or REVERSE LOOP TEST.

(b) The selected operation mode is stored in M9240 and M9252.

(2) Communication status of the station itself

(a) Displays the communication status of the host local station itself.

1) P-MTR WAITING:

Awaiting parameter data to be sent from the master station.

2) OK: Normal communication is being executed.

3) STOP:

The local station itself is disconnected and communication has been stopped.

(b) The current communication status is stored in M9250 and M9251.

(3) Loop line status of the station itself

(a) Displays the forward loop (F loop) and reverse loop (R loop) status of the local station itself.

Only OK is displayed when a MELSECNET/B Data Link System is used.

1) OK: Loop line is normal.

2) NG: Loop line is faulty.

(b) The loop line status is stored in M9241 and M9242.

(4) Loopback execution status

(a) Displays whether loopback has been executed by the local station itself.

1) OK (executed):

Loopback has been executed by the local station itself.

2) NG (not executed):

Loopback has not been executed by the local station itself.

(b) The loopback execution status is stored in M9243.

(5) B/W/Y receive status

(a) Displays whether the link relays (B), link registers (W), and link outputs (Y) are being received from the master station.

1) OK (receiving):

B, W, and Y are being received from the master station in the cyclic communication mode.

2) NG (not receiving):

The local station itself is disconnected and B, W, and Y are not being received from the master station.

(b) The B/W/Y receive status is stored in M9246.

(6) B/W receive status (local station in three-tier system)

(a) Displays whether a local station in the third tier is receiving the link relays (B) and link registers (W) from the master station for the second tier.

1) OK (receiving):

B and W are being received from the master station for the second tier in the cyclic communication mode.

2) NG (not receiving):

The local station itself is in a status in which B and W are not being received from the master station for the second tier. Reception will be disabled when M9247 is turned ON.

(b) The B/W receive status is stored in M9247.

(7) Local station operation status

(a) Displays the operation status of the local station.

1) RUN : Station in RUN status
2) STOP : Station in STOP status
3) DOWN : Station is disconnected from the link

(b) The operation status of remote I/O stations will always be RUN.

(c) The data of local station operation status is stored in D9248 to D9251 and D9252 to D9255.

(This data is the same as the data in D9248, D9249, D9252, and D9253 when a MELSECNET/B Data Link System is used.)

5.1.3 Remote I/O station link monitor

This section describes the link monitor data for the following two link monitor functions:

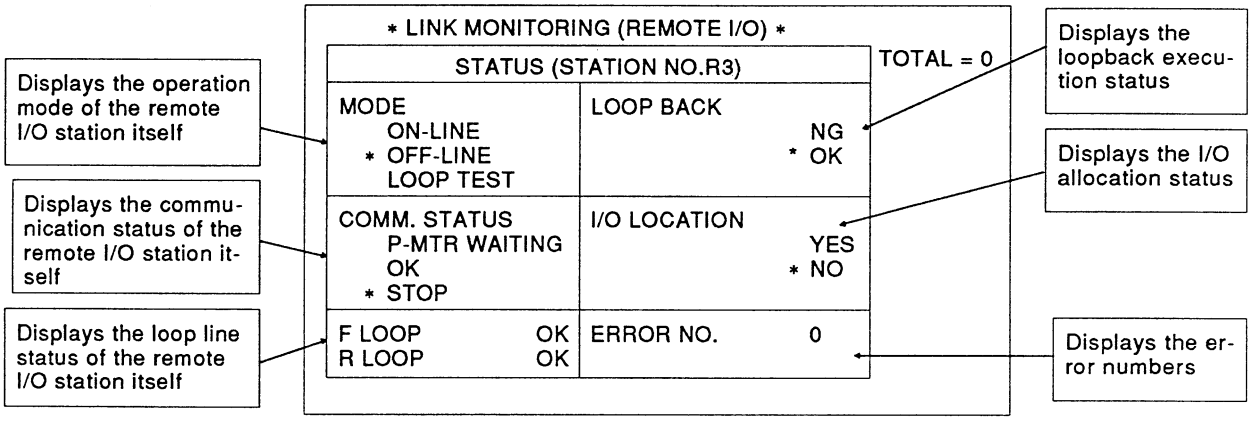
(a) Loop monitor:

The data link status of the remote I/O station itself.

(b) Batch monitor:

The data link status of the devices that are sent/received by the remote I/O stations themselves (batch monitored).

[Loop Monitor]



(1) Operation mode of the station itself

(a) Displays the remote I/O station operation status

1) ONLINE:

Remote I/O station mode setting is ONLINE (automatic return function set/not set).

2) OFFLINE:

Remote I/O station mode setting is OFFLINE, SELF-LOOPBACK TEST, or STATION-TO-STATION TEST.

3) LOOP TEST:

Remote I/O station mode setting is FORWARD LOOP TEST or REVERSE LOOP TEST.

(2) Communication status of the station itself

(a) Displays the communication status of the remote I/O station itself.

1) P-MTR WAITING:

Awaiting parameter data to be sent from the master station.

2) OK: Normal communication is being executed.

3) STOP:

The remote I/O station itself is disconnected and communication has been stopped.

(3) Loop line status of the station itself

(a) Displays the forward loop (F loop) and reverse loop (R loop) status of the remote I/O station itself.

1) OK: Loop line is normal.

2) NG: Loop line is faulty.

(4) Loopback execution status

(a) Displays whether loopback has been executed by the remote I/O station itself.

1) OK (executed):

Loopback has been executed by the remote I/O station itself.

2) NG (not executed):

Loopback has not been executed by the remote I/O station itself.

(5) I/O allocation status

(a) Displays whether I/O allocation has been performed by the master station.

1) YES:

I/O allocation has been performed by the master station.

2) NO:

I/O allocation has not been performed by the master station.

(6) Error numbers

Error Number	Error Description	Counter Measure
10	A special function module loaded to a remote I/O station does not occupy 32 points.	Remove the special function modules that do not occupy 32 I/O points.
11	Special function module hardware error.	Replace the special function module.
12	The number of words read by an RFRP instruction exceeds the link register (W) range specified with the link parameters.	• Change the link register (W) range set with the link parameters. • Change the number of words to be read by an RFRP instruction.
13	The number of words written by an RTOP instruction exceeds the link register (W) range specified with the link parameters.	• Change the link register (W) range set with the link parameters. • Change the number of words to be read by an RTOP instruction.
14	An RFRP instruction has been executed when a special function module was faulty.	Special function module hardware error.
15	An RTOP instruction has been executed when a special function module was faulty.	Special function module hardware error.
20	Blown fuse in the I/O module.	Replace the fuse in the I/O module loaded to the remote I/O station.
21	I/O module verify error (The I/O module data in the remote I/O station is different from the data recognized when the power was turned ON.) (1)The I/O module is not secure. (2) The I/O module has been removed or another I/O module has been loaded during operation.	• Check or replace the I/O module. • Reset the master station or the remote I/O station.
22	Neither inputs (X) nor outputs (Y) have been specified with the parameters.	Check the I/O modules in the remote I/O station and set the parameters again.
23	I/O allocation error.	Check the link allocation for the I/O modules and the master station and correct the I/O allocation.
24	Remote I/O station specification error.	Check if the remote I/O station number is set with the link parameters as a local station and correct the setting.

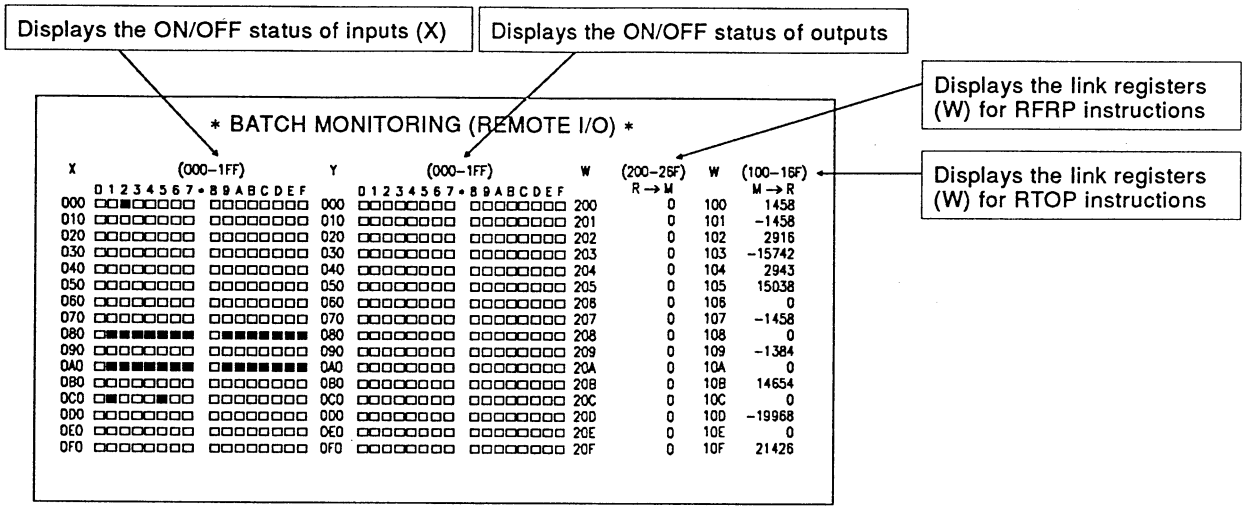
(7) Station number

Displays the station number of the remote I/O station to which the GPP is connected.

(8) Number of slave stations

Displays the total number of local and remote I/O stations connected in the loop.

[Batch Monitor]



(1) ON/OFF status of inputs (X)

(a) Displays the ON/OFF status of inputs (X) sent from a remote I/O station to the master station.

1) ■ : ON status

2) □ : OFF status

(b) If the remote I/O station is online, the device numbers at the master station are used for the display.

If the remote I/O station is offline, the device numbers at the host remote I/O station are used for the display.

(2) ON/OFF status of outputs (Y)

(a) Displays the ON/OFF status of outputs (Y) sent from the master station to a remote I/O station.

1) ■ : ON status

2) □ : OFF status

(b) If the remote I/O station is online, the device numbers at the master station are used for the display.

If the remote I/O station is offline, the device numbers at the remote I/O station itself are used for the display.

(3) Link registers (W) for RFRP instructions

(a) Displays the data in the area set for data transmission from the remote I/O station itself to the master station.

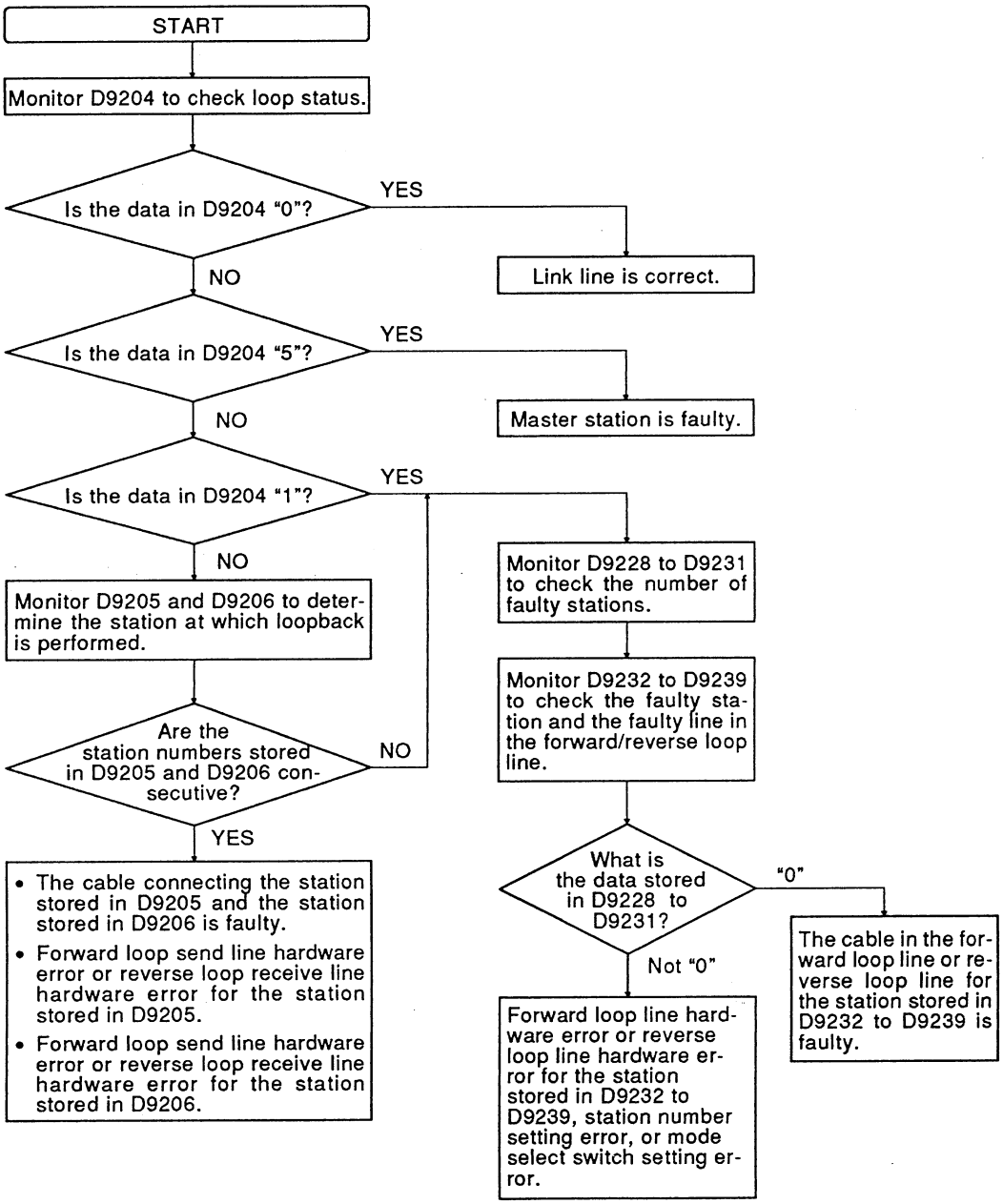
(4) Link registers (W) for RTOP instructions

(a) Displays the data in the area set for data transmission from the master station to the remote I/O station itself.

5.2 Monitoring the Special Relays and Special Registers Used for the Link

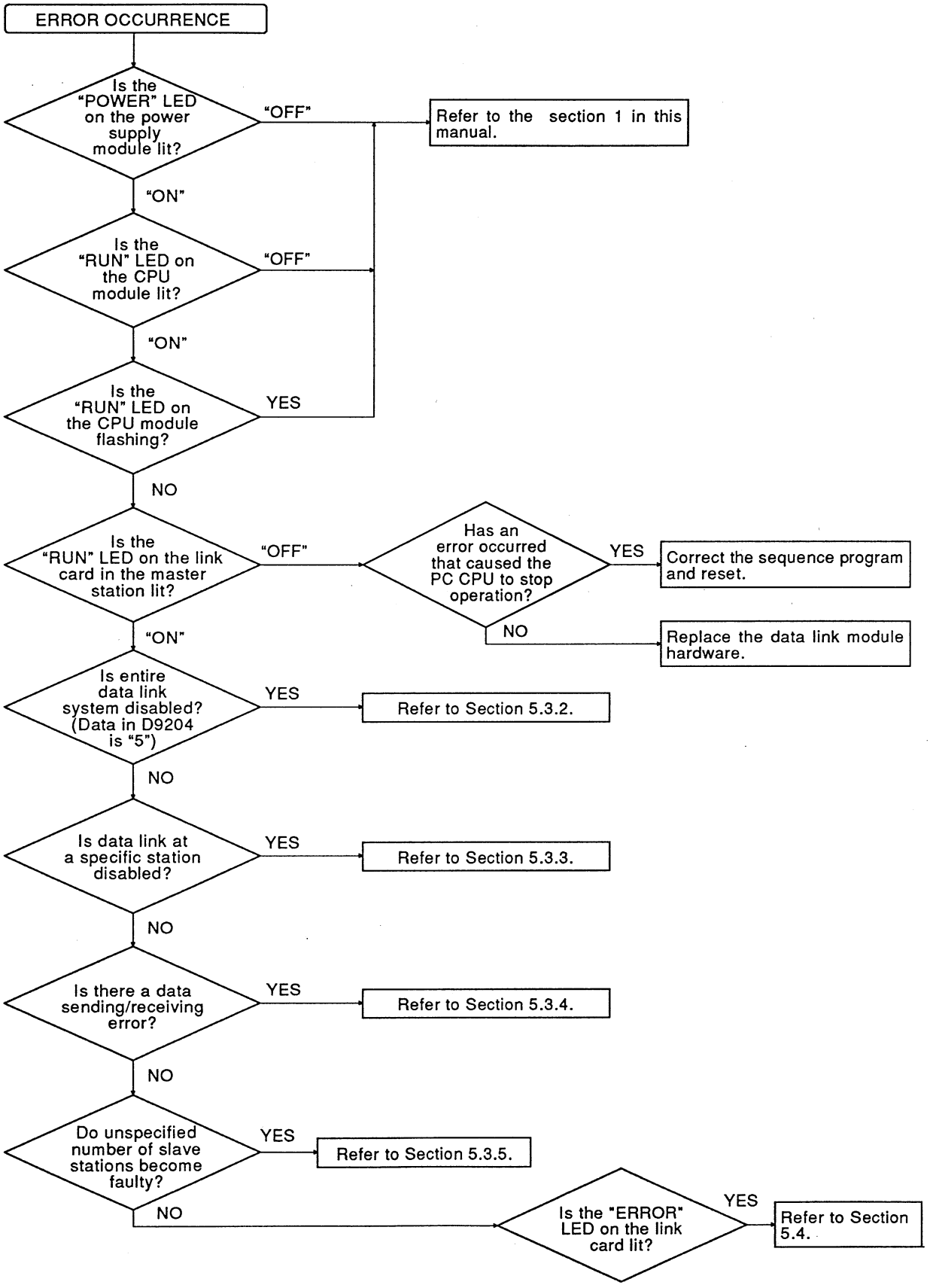
Faulty stations in the MELSECNET Data Link System can be found by using an A7PU to monitor the special relays and special registers used for the link. When a A6GPP/A6PHP is available, use the link monitoring function as explained in Section 10.1.

Refer to Sections 1.3.5 and 1.3.6 for details on special relays and special registers.

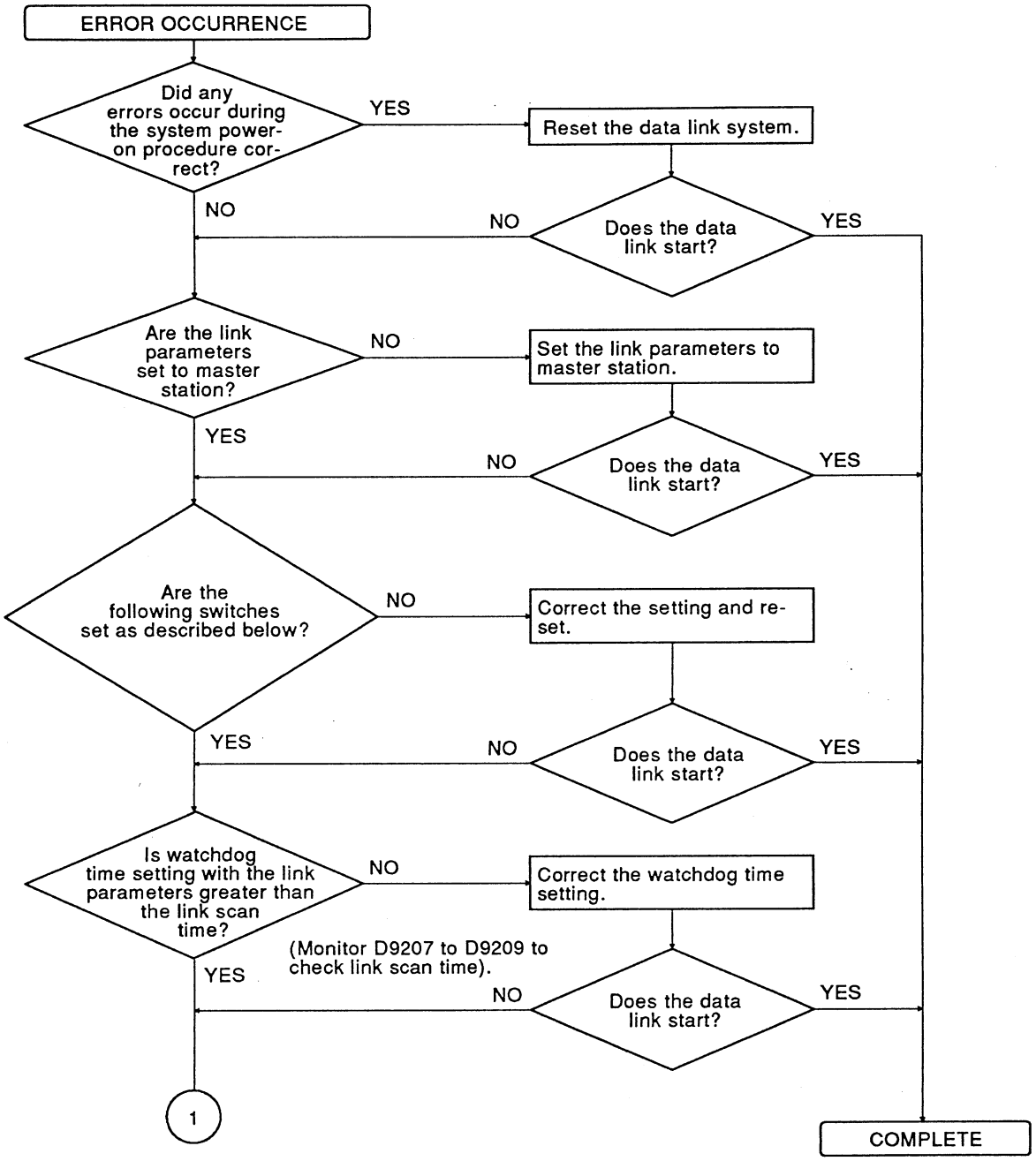


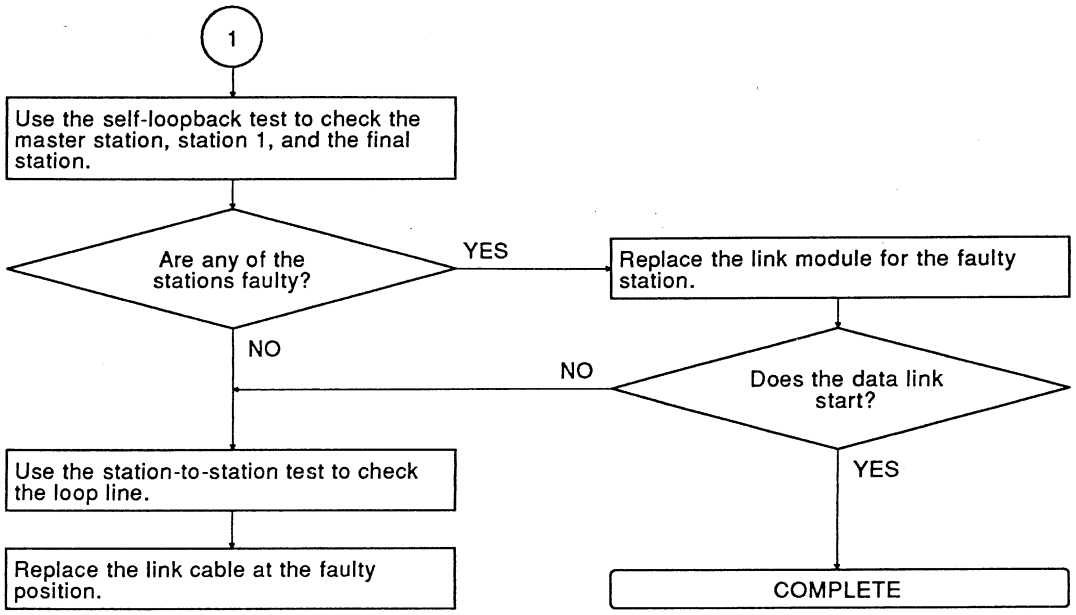
5.3 Troubleshooting Flow Chart

5.3.1 General troubleshooting flow chart



5.3.2 Troubleshooting flow chart for when the data link is disabled throughout the entire system



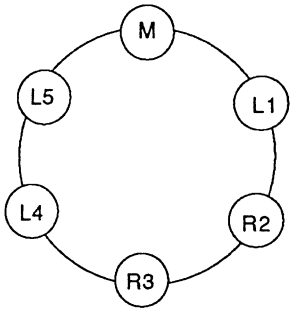


POINT

If the power supplies of the local and/or remote I/O stations on either side of a normally operating local or remote I/O station are turned off simultaneously (within 100 msec), the data link for the entire system might be disabled.

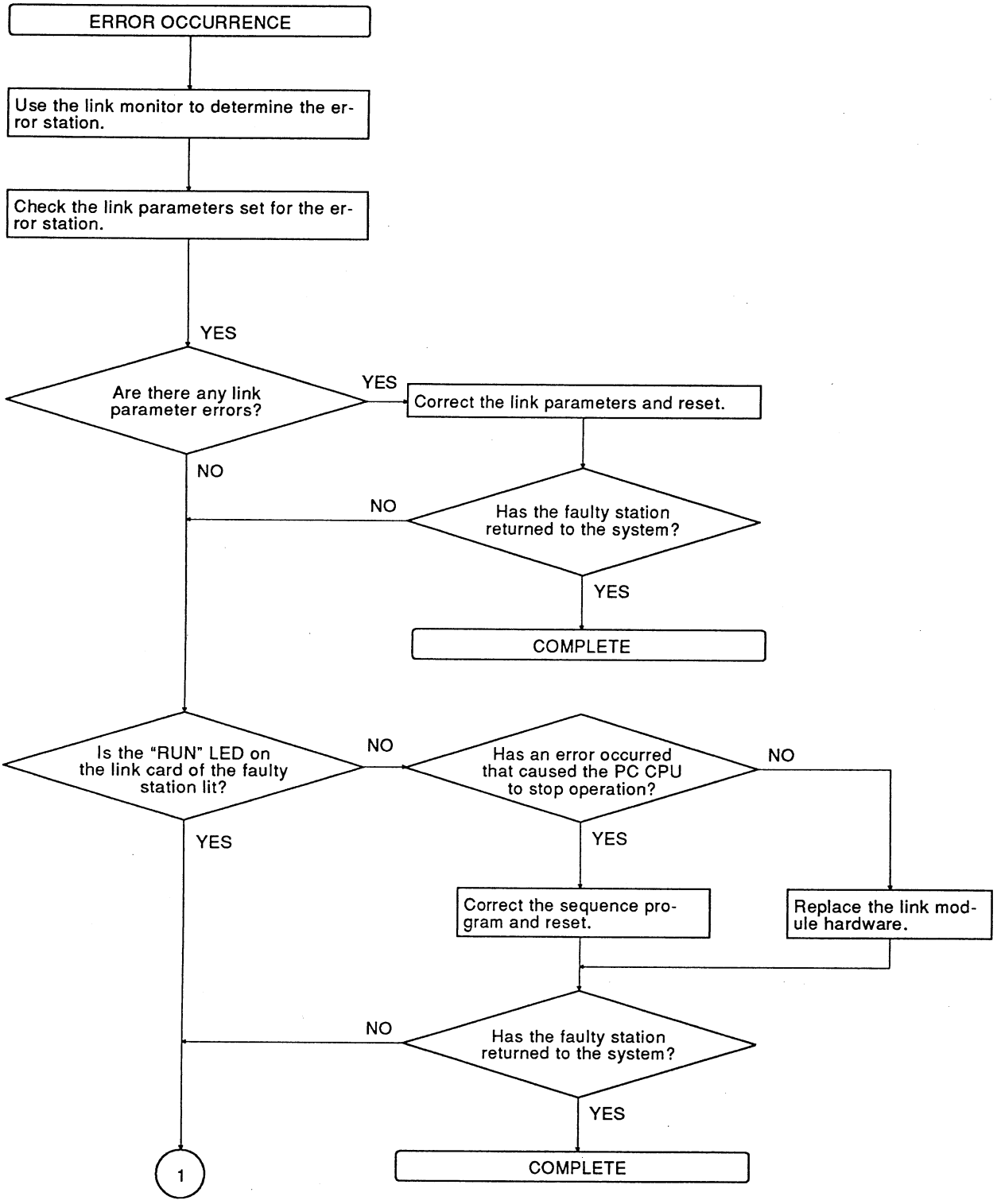
If the automatic return function is set for these stations, data communication resumes immediately. However, if the automatic return function is not set for these stations, they will remain disconnected. The CPU for each disconnected station must be reset in order to return them to the data link.

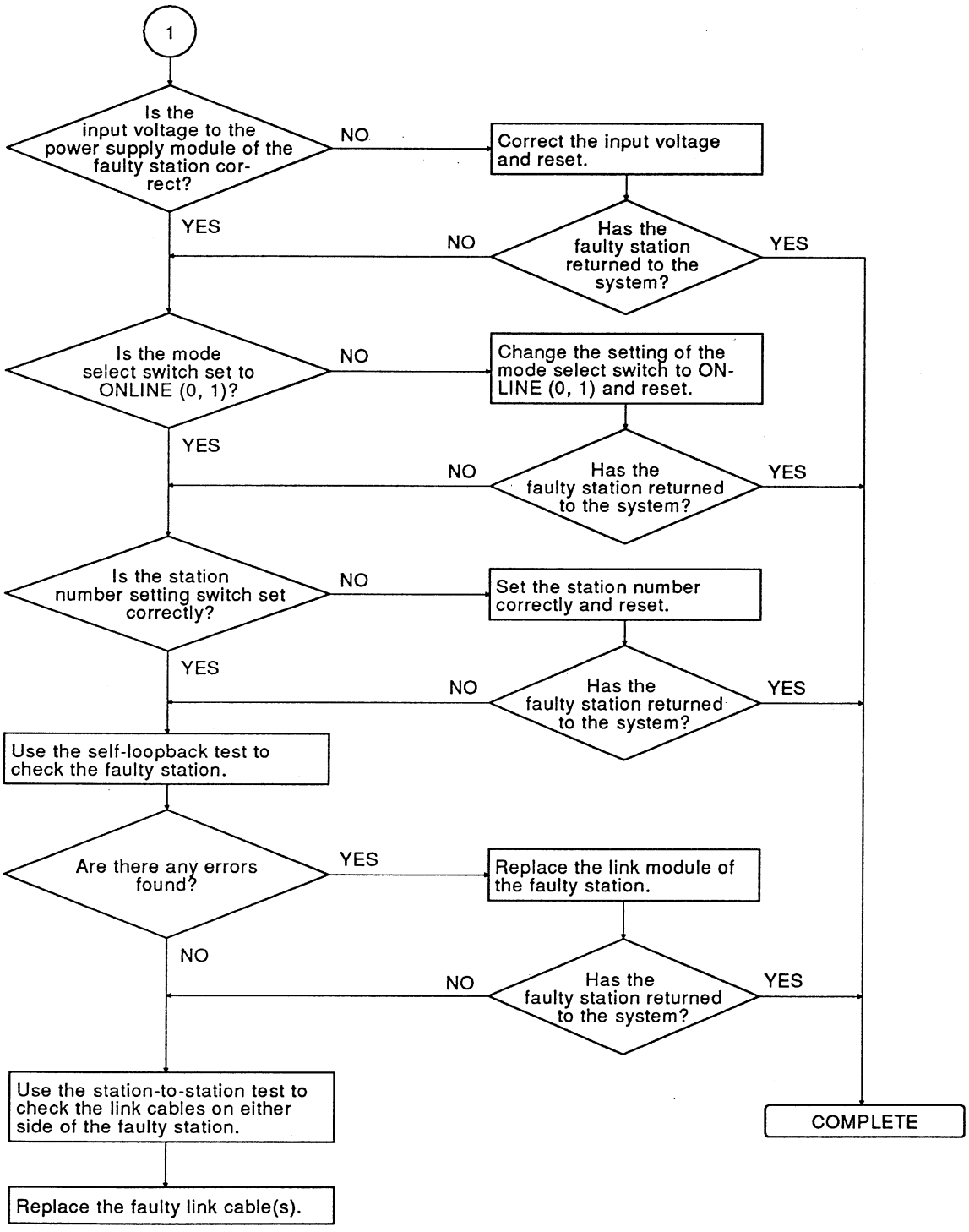
Example:



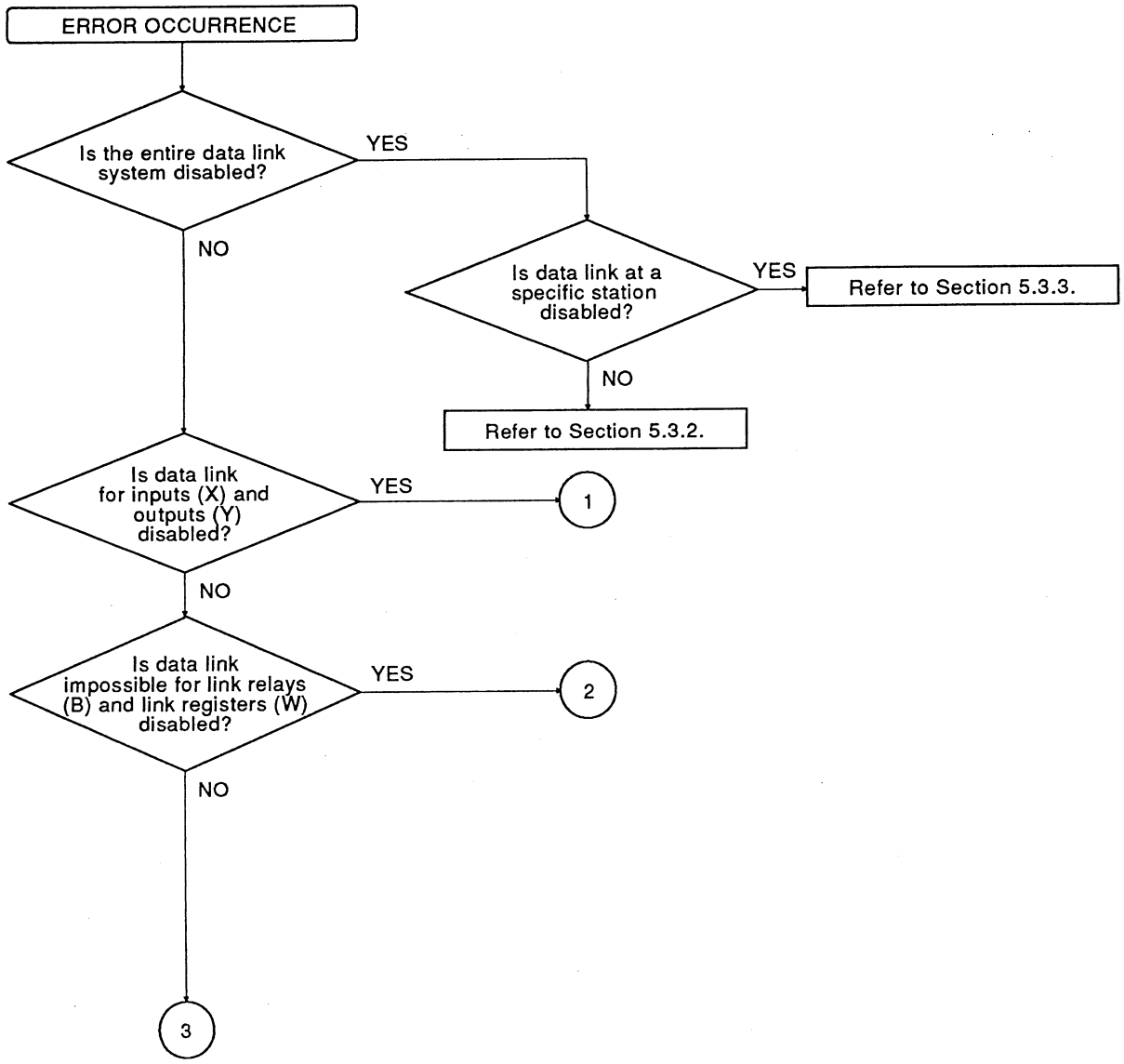
If power supply to L1 and R3 is turned off simultaneously (within 100 msec) while R2 is operating normally, the data link for the entire system might be disabled.

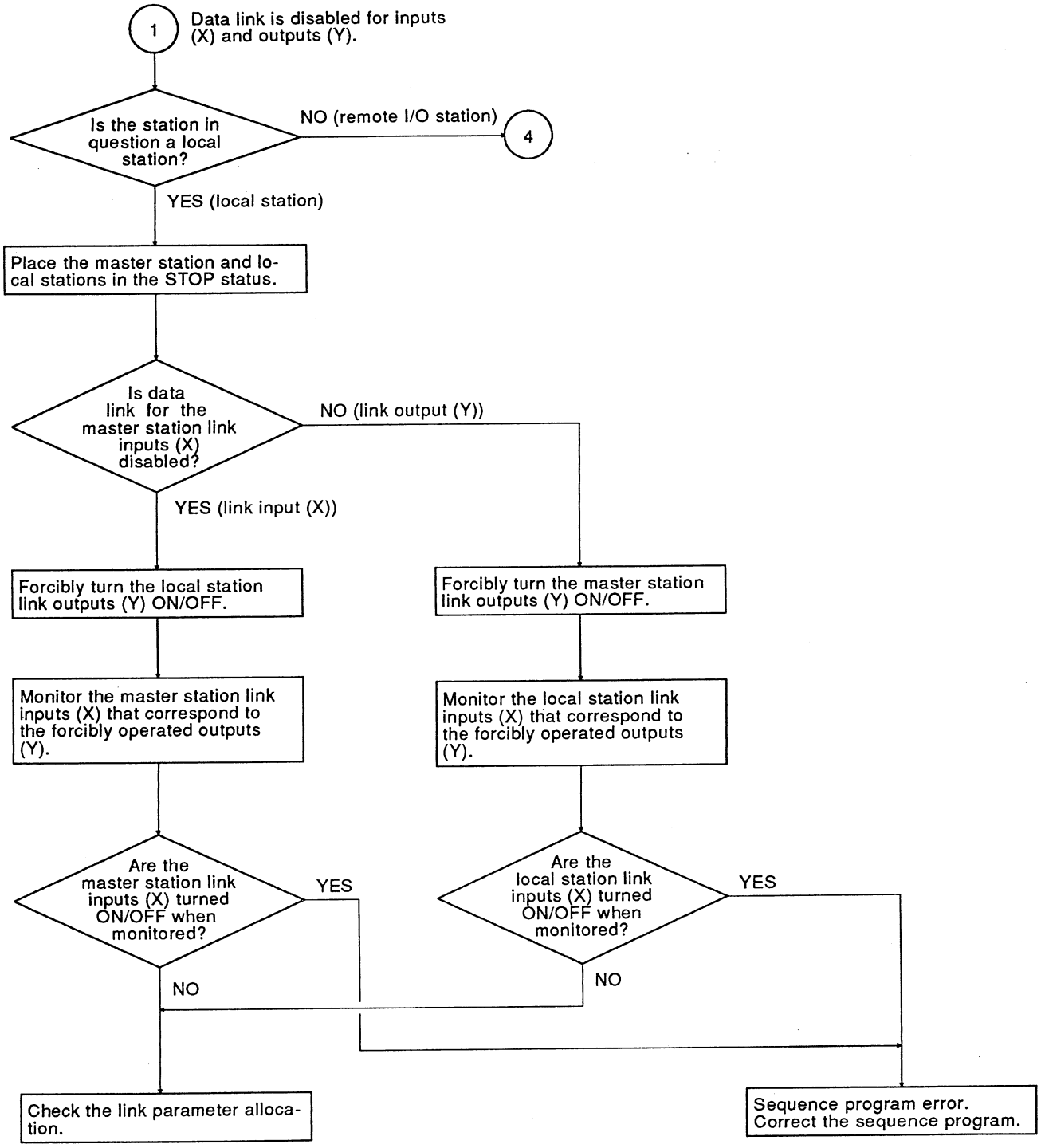
5.3.3 Troubleshooting flow chart for when the data link is disabled at a specific station

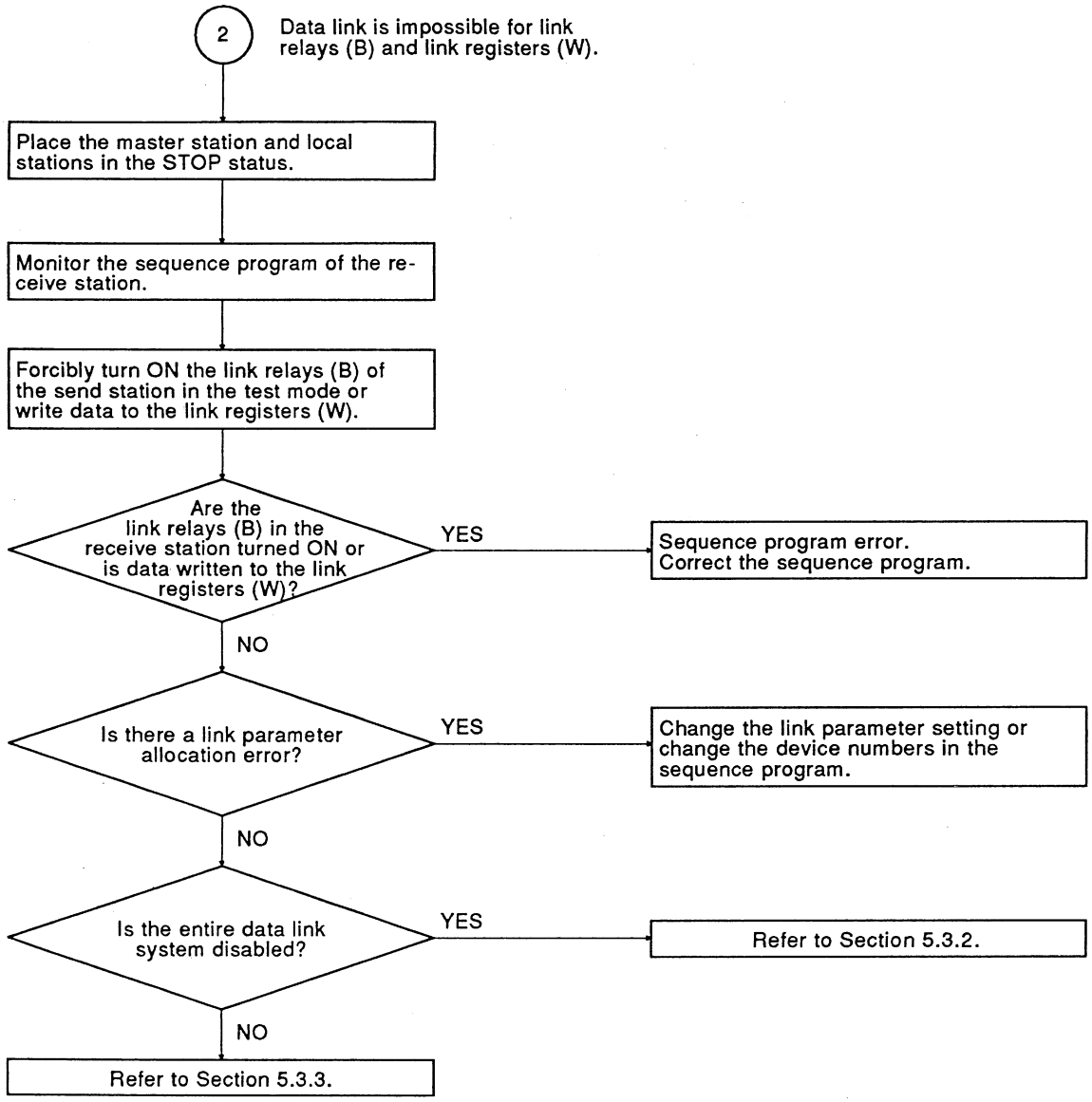


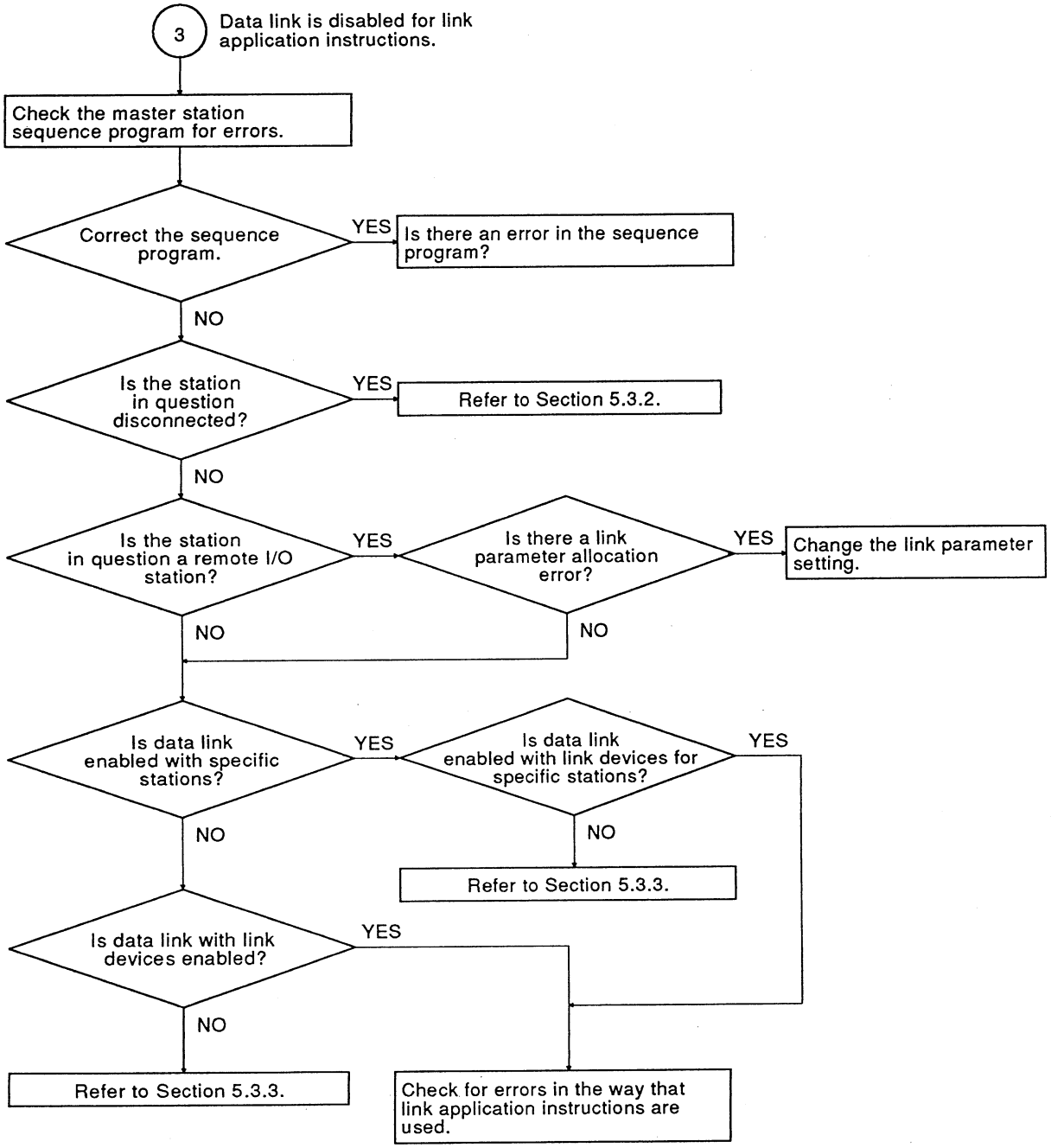

1
Is the input voltage to the power supply module of the faulty station correct?
NO
Correct the input voltage and reset.
YES
NO
Has the faulty station returned to the system?
YES
Is the mode select switch set to ONLINE (0, 1)?
NO
Change the setting of the mode select switch to ONLINE (0, 1) and reset.
YES
NO
Has the faulty station returned to the system?
YES
Is the station number setting switch set correctly?
NO
Set the station number correctly and reset.
YES
NO
Has the faulty station returned to the system?
YES
Use the self-loopback test to check the faulty station.
Are there any errors found?
YES
Replace the link module of the faulty station.
NO
NO
Has the faulty station returned to the system?
YES
Use the station-to-station test to check the link cables on either side of the faulty station.
COMPLETE
Replace the faulty link cable(s).

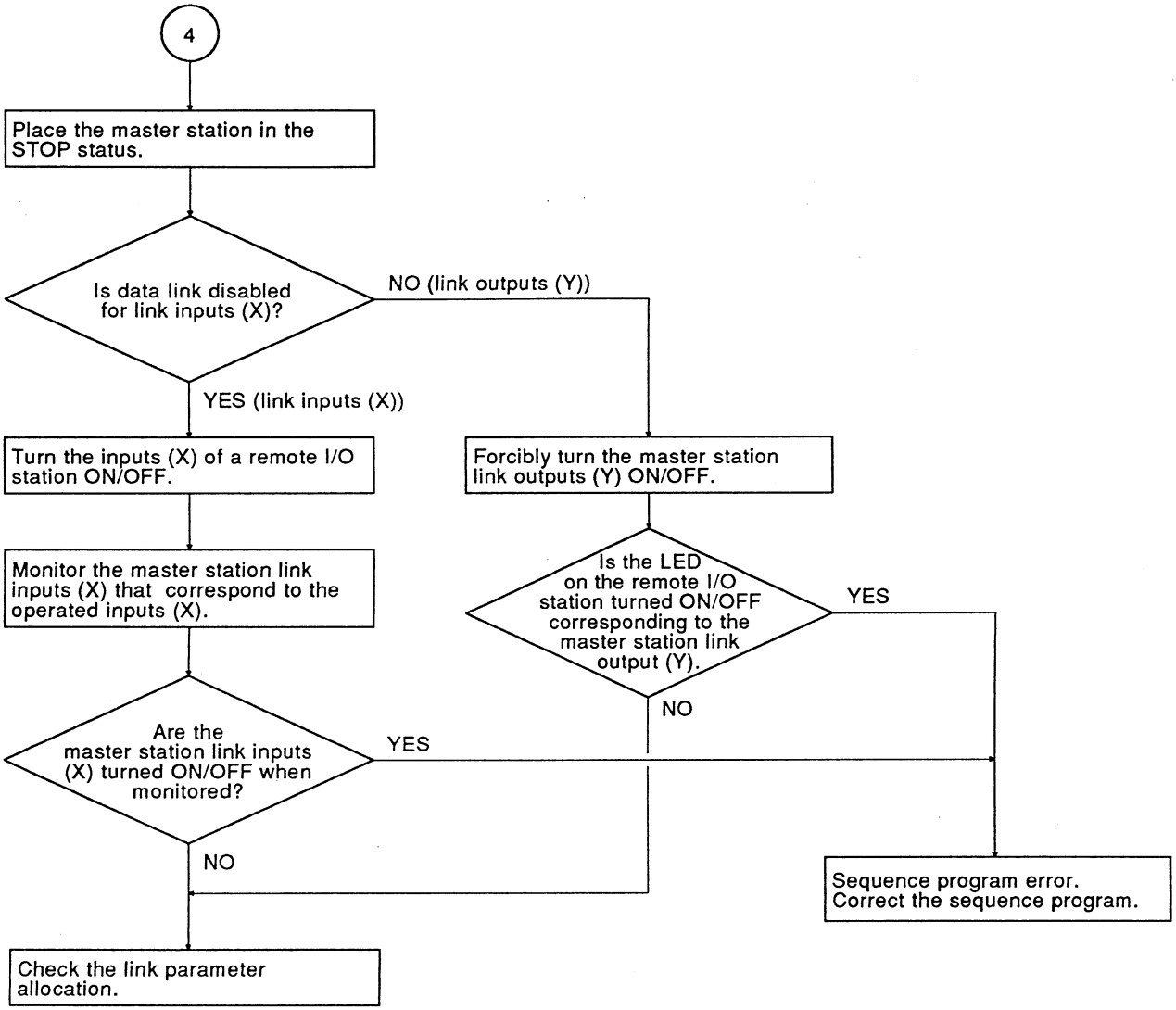
5.3.4 Troubleshooting flow chart for when a data send/receive error occurs



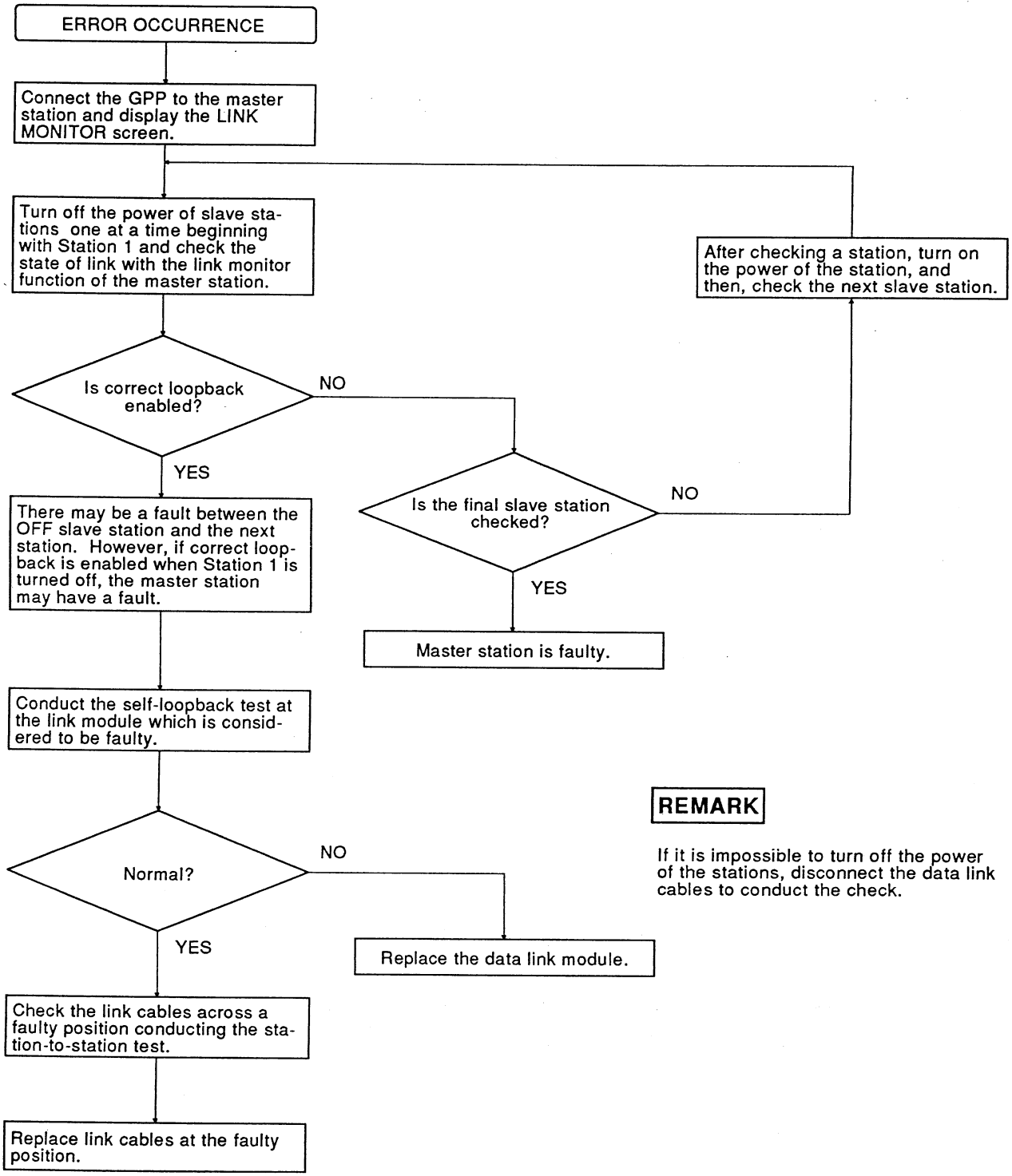

1
Data link is disabled for inputs (X) and outputs (Y).
Is the station in question a local station?
NO (remote I/O station)
4
YES (local station)
Place the master station and local stations in the STOP status.
Is data link for the master station link inputs (X) disabled?
NO (link output (Y))
YES (link input (X))
Forcibly turn the local station link outputs (Y) ON/OFF.
Forcibly turn the master station link outputs (Y) ON/OFF.
Monitor the master station link inputs (X) that correspond to the forcibly operated outputs (Y).
Monitor the local station link inputs (X) that correspond to the forcibly operated outputs (Y).
Are the master station link inputs (X) turned ON/OFF when monitored?
YES
Are the local station link inputs (X) turned ON/OFF when monitored?
YES
NO
NO
Check the link parameter allocation.
Sequence program error. Correct the sequence program.


2
Data link is impossible for link relays (B) and link registers (W).
Place the master station and local stations in the STOP status.
Monitor the sequence program of the receive station.
Forcibly turn ON the link relays (B) of the send station in the test mode or write data to the link registers (W).
Are the link relays (B) in the receive station turned ON or is data written to the link registers (W)?
YES
Sequence program error. Correct the sequence program.
NO
Is there a link parameter allocation error?
YES
Change the link parameter setting or change the device numbers in the sequence program.
NO
Is the entire data link system disabled?
YES
Refer to Section 5.3.2.
NO
Refer to Section 5.3.3.


3
Data link is disabled for link application instructions.
Check the master station sequence program for errors.
Correct the sequence program.
YES
Is there an error in the sequence program?
NO
Is the station in question disconnected?
YES
Refer to Section 5.3.2.
NO
Is the station in question a remote I/O station?
YES
Is there a link parameter allocation error?
YES
Change the link parameter setting.
NO
NO
Is data link enabled with specific stations?
YES
Is data link enabled with link devices for specific stations?
YES
NO
NO
Refer to Section 5.3.3.
Is data link with link devices enabled?
YES
NO
Refer to Section 5.3.3.
Check for errors in the way that link application instructions are used.


4
Place the master station in the STOP status.
Is data link disabled for link inputs (X)?
NO (link outputs (Y))
YES (link inputs (X))
Turn the inputs (X) of a remote I/O station ON/OFF.
Forcibly turn the master station link outputs (Y) ON/OFF.
Monitor the master station link inputs (X) that correspond to the operated inputs (X).
Is the LED on the remote I/O station turned ON/OFF corresponding to the master station link output (Y).
YES
NO
Are the master station link inputs (X) turned ON/OFF when monitored?
YES
NO
Sequence program error. Correct the sequence program.
Check the link parameter allocation.

5.3.5 Troubleshooting flow chart for when unspecified number of slave stations become faulty

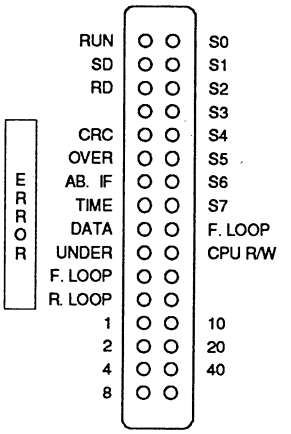


REMARK

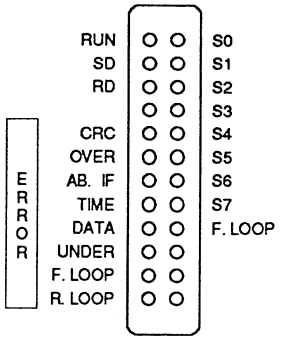
If it is impossible to turn off the power of the stations, disconnect the data link cables to conduct the check.

5.4 Error LED

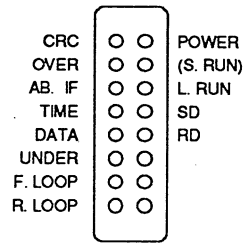
This section explaings an LED to be lighted when an error occurs in the LED on the front of data link unit.



Building block CPU21/R21



AJ71P22/R22
AJ72P25/R25
AJ71P21/R21



A0J2CPUP23/R23
A0J2P25/R25
A0J2HCPUP21/R21

Display	Error Name	Error Detection Status	Possible Causes
CRC	CRC error (cyclic redundancy check)	ON	• The code of received data is checked. • This error might occur depending on the timing in which the station sending the data is disconnected from the link. • Cable fault, noise, etc. caused the error.
OVER	Overrun error	ON	• A set of received data has overwritten the previous set of data before it was processed. • A hardware error with the data link module receive circuit has occurred. • Note: In a system in which local stations and remote I/O stations are connected, the "OVER" LED on the remote I/O station will be lit dimly when there is no error.
AB.IF	Abort invalid frame error	ON	• "1" bits are received continuously and the limit is exceeded or the length of received data is shorter than the specified length. • This error might occur depending on the timing in which the station sending the data is disconnected from the link. • Short watchdog time setting, cable fault, noise, etc. caused the error.
TIME	Time check error	ON	• The data link watchdog timer in the master station operates. An error has occurred at a local station or a remote I/O station. • Short watchdog time setting, cable fault, noise, etc. caused the error.
DATA	Data check error	ON	• Error code data is received (can only be lit in the test mode). • Cable fault, noise, etc. caused the error.
UNDER	Underrun error	ON	• Send data internal processing is not being performed at regular intervals. • A hardware error with the data link module send circuit has occurred.
F.LOOP	Forward loop error	ON	• The forward loop line has a fault or the power supply to the adjacent stations has been turned off. • The forward loop line cable is broken or not connected.
R.LOOP	Reverse loop error	ON	• The reverse loop line has a fault or the power supply to the adjacent stations has been turned off. • The reverse loop line cable is broken or not connected.

5.5 Link Special Relay and Special Register

It is recommended to provide an interlock to stop execution of a program immediately when an error occurs by using these special relays and a special register in the sequence program from a failsafe point of view.

5.5.1 MELSECNET data link

(1) Special link relays

1) Special link relays effective only for the master station

Device Number	Name	Data	Description
M9200	LRDP instruction received	OFF : Unreceived ON : Received	• Turned ON when an LRDP (word device read) instruction is received. • Used in a user program as an interlock for an LRDP instruction. • Remains ON after the completion of word device read processing called by an LRDP instruction. Turned OFF with an RST instruction in a user program.
M9201	LRDP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON after an LRDP (word device read) instruction has been executed. The execution results are stored in D9200. • Used as a conditional contact to reset M9200 and M9201 after the completion of word device read processing called by an LRDP instruction. • Turned OFF with an RST instruction in a user program after it has been turned ON.
M9202	LWTP instruction received	OFF : Unreceived ON : Received	• Turned ON when an LWTP (word device write) instruction is received. • Used in a user program as an interlock for an LWTP instruction. • Remains ON after the completion of word device write processing called by an LWTP instruction. Turned OFF with an RST instruction in a user program.
M9203	LWTP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON after an LWTP (word device write) instruction has been executed. The execution results are stored in D9201. • Used as a conditional contact to reset M9202 and M9203 after the completion of word device write processing called by an LWTP instruction. • Turned OFF with an RST instruction in a user program after it has been turned ON.
M9206	Link parameter error in the station itself	OFF : Normal ON : Error	• Turned ON when link parameter of the station itself is not set or the setting is incorrect. • Automatically turned OFF when link parameter is set correctly.
M9207	Link parameter check result	OFF : Normal ON : Error	• Goes ON if a lower tier link uses device ranges (B, W) outside the range set by a master station, in the upper tier link, for itself. • Check is executed only when M9209 is ON.
M9208	B and W transmission range for the master station (lower tier master stations only)	OFF : To the second and third tiers ON : To the second tier only	• Sets whether the B and W data controlled by the master station in the upper tier is sent to the local stations (sub-slave stations) in the lower tier. • OFF : B and W data in the master station is sent to the sub-slave stations. • ON : B and W data in the master station is not sent to the sub-slave stations.

Device Number	Name	Data	Description
M9209	Link parameter check instruction (lower tier link master stations only)	OFF : Check executed ON : Check not executed	• To be turned ON when the link devices (B and W) used by the upper tier and the link devices (B and W) used by the lower tier are not compared for "match". • When M9209 is OFF, the link parameters for the upper tier and the link parameters for the lower tier are checked.
M9210	Link card error (master station)	OFF : Normal ON : Error	• Turned ON when the link card hardware is faulty.
M9224	Link status	OFF : Offline ON : Online, station-to-station test, or self-loopback test	• Turned ON when the master station is offline, in the station-to-station test mode, or in the self-loopback test mode. • Turned OFF when the master station is reset after being placed in the online mode.

M9225	Forward loop error	OFF : Normal
		ON : Error
			• Turned ON when any of the following occurs in the forward loop line between the master station and the final station:
			  • Broken cable
			  • Forward loop receive end error in the master station data link module
			  • Forward loop send end error in the data link module of the final local station
			• Turned ON when the station-to-station test, including the final station, is executed during the data link.
			• Turned OFF automatically when the error state is eliminated.

M9226	Reverse loop error	OFF : Normal
		ON : Error
			• Turned ON when any of the following occurs in the forward loop line between the master station and the final station 1:
			  • Broken cable
			  • Reverse loop receive end error in the master station data link module
			  • Reverse loop send end error in the data link module of the final local station
			• Turned ON when the station-to-station test, including station 1, is executed during the data link.
			• Turned OFF automatically when the error state is eliminated.

M9227	Loop test status	OFF : Not being executed ON : Forward loop test or reverse loop test being executed	• Turned ON when a forward loop test or reverse loop test is being executed for the master station.
M9232	Local station operating status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of the local station. • Turned ON when the status of any local station in the loop changes to STOP or PAUSE. • Turned OFF automatically when the status of all local stations changes to RUN or STEP RUN. That is, M9232 is turned OFF when bits D9212 to D9215 are all OFF.
M9233	Local station error detected	OFF : No error ON : Error detected	• Turned ON when a local station in the executed loop detects an error in another station (M9255 ON). • Turned OFF automatically when the faulty station is returned to the normal state or the data link returns to the normal status by switching the loop line. That is, M9233 is turned OFF when bits D9216 to D9219 are all OFF.

Device Number	Name	Data	Description
M9235	Local station or remote I/O station parameter error detected	OFF : No error ON : Error detected	• Turned ON in the following cases: Local station : The device range (link relays and link registers) outside the range allocated to the master station in the lower tier is allocated with the link parameters for the lower tier. Remote I/O station : Error in I/O allocation or neither inputs (X) nor outputs (Y) are set with the link parameters. • Turned OFF when the error is eliminated by correcting the link parameters. That is, M9235 is turned OFF when bits D9220 to D9223 are all OFF.
M9236	Local station or remote I/O station initial communication status	OFF : Not communicating ON : Communicating	• Turned ON while a local station and/or remote I/O station is communicating the initial setting data (link parameter) to the master station to execute data link processing. • Automatically turned OFF when the communication for initial data setting has been completed. That is, M9236 is turned OFF when bits D9224 to D9227 are all OFF.
M9237	Local station or remote I/O station error	OFF : Normal ON : Error	• Turned ON when an error occurs with one local station or remote I/O station within the loop. (The relay is turned ON while a station-to-station test is being executed for a local station or a remote I/O station and the data link is operating.) • Automatically turned OFF when the faulty station returns to the normal status or the data link returns to the normal status by switching the loop line. That is, M9237 is turned OFF when bits D9228 to D9231 are all OFF.
M9238	Local station or remote I/O station forward/reverse loop error	OFF : Normal ON : Error	• Turned ON when an error occurs in the forward loop line or reverse loop line of the local stations and remote I/O stations. That is, M9238 is turned OFF when bits D9232 to D9239 are all OFF.

2) Special link relays effective only for local stations

Device Number	Name	Data	Description
M9204	LRDP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON by a local station upon the completion of word device read processing called by an LRDP instruction.
M9205	LWTP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON by a local station upon the completion of word device write processing called by an LRDP instruction.
M9211	Link card error (local station)	OFF : Normal ON : Error	• Turned ON when the link card hardware is faulty.
M9240	Link status	OFF : Online ON : Offline, station-to-station test, or self-loopback test	• Turned ON when the station itself is offline, in the station-to-station test mode, or in the self-loopback test mode. • Turned OFF when the station itself is reset after being placed in the online mode.

M9241	Forward loop error	OFF : Normal
		ON : Error
			• Turned ON when any of the following occurs in the forward loop line between the station itself and the preceding station:
			  • Broken cable
			  • Forward loop receive end error in the station itself data link module
			  • Forward loop send end error in the data link module of the proceding station
			• Turned OFF automatically when the error state is elimnated.

M9242	Reverse loop error	OFF : Normal
		ON : Error
			• Turned ON when any of the following occurs in the reverse loop line between the station itself and the next station:
			  • Broken cable
			  • Reverse loop receive end error in the data link module of the station itself
			  • Reverse loop send end error in the data link module of the next station
			• Turned OFF automatically when the error state is elimnated.

M9243	Loopback executed	ON : Not-executed OFF : Executed	• Turned ON when loopback is executed by the station itself.
M9246	Data unreceived	OFF : Received ON : Unreceived	• Turned ON when the data from the master station has not been received.
M9247	Data unreceived	OFF : Received ON : Unreceived	• In the three-tier system, M9247 is turned ON when the data from the master station for the third tier has not been received by a sub-slave station. That is, M9247 is ON while M9208 is ON.
M9250	Parameter unreceived	OFF : Received ON : Unreceived	• Turned ON when the link parameters have not been received from the master station. • Automatically turned OFF when the link parameter is received. • The master station sends the link parameters to each local station every time the loop line is switched. • Only effective while the loop line in which the data link is executed is online.
M9251	Link break	OFF : Normal ON : Break	• ON/OFF status depends on whether the station itself stopped the data link. • Turned ON when the data link is established in neither the forward loop line nor the reverse loop line. • Turned OFF automatically when the data link returns to the normal state. • Only effective while the loop line in which the data link is executed is online.

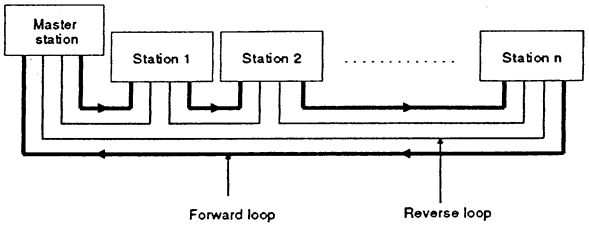
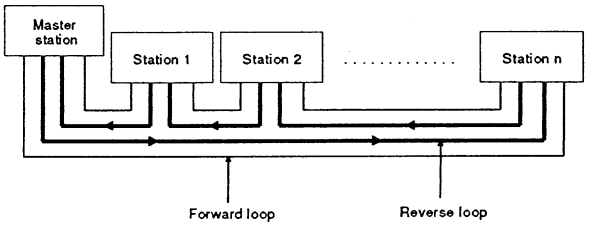
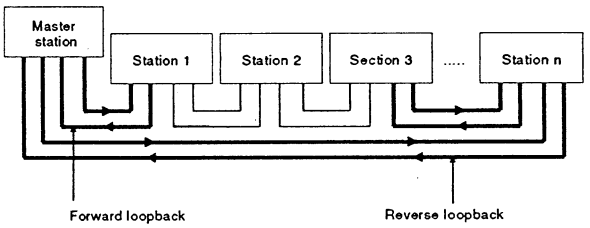
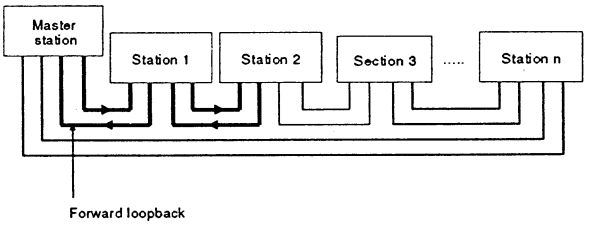
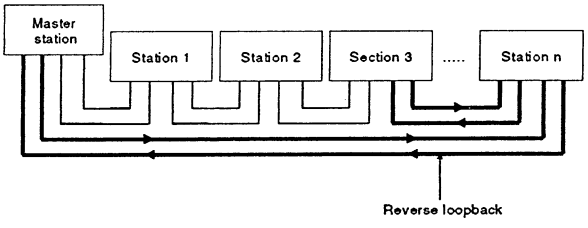
Device Number	Name	Data	Description
M9252	Loop test status	OFF : Not executed ON : Forward loop test or reverse loop test is being executed.	• Remains ON while the station itself is in the forward loop test mode or the reverse loop test mode.
M9253	Master station operating status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of the master station. • Turned ON when the status of a master station is either STOP or PAUSE. • Turned OFF when the status of the master station changes to RUN or STEP RUN.
M9254	Operating status of other local stations	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of a local station other than the station itself. • Turned ON when the status of a local station in the loop (other than the station itself) is either STOP or PAUSE. • Not turned ON when the status of the station itself is either STOP or PAUSE. • Automatically turned OFF when the status of a local station in the loop (other than the station itself) changes to RUN or STEP RUN.
M9255	Error status of other local stations	OFF : Normal ON : Error	• ON/OFF status depends on the operation status of a local station other than the station itself. • Turned ON when an error occurs with one local station in the loop (other than the station itself). • Automatically turned OFF when the faulty station returns to the normal state or the data link returns to the normal state by switching the loop line. That is, M9255 is turned OFF when bits D9252 to D9255 are all OFF.

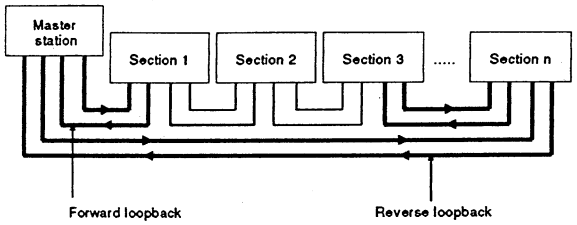
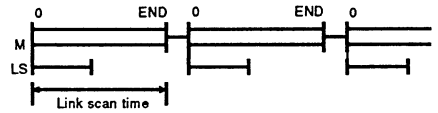
(2) Special link registers

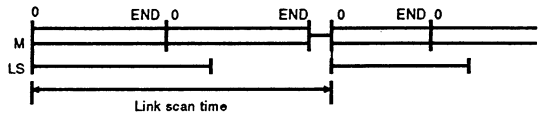
1) Special link registers effective only for the master station

Device Number	Name	Data	Description
D9200	LRDP execution result	0 : Normal 2 : LRDP instruction setting fault 3 : Corresponding station error 4 : LRDP cannot be executed in the corresponding station	Stores the execution result of an LRDP (word device read) instruction (M9201 ON). • LRDP instruction setting fault: Faulty setting of the LRDP instruction constant, source, and/or target. • Corresponding station error: The designated station is not executing data link processing. • LRDP instruction cannot be executed by thecorrespopnding station:thestation designated with the LRDP instruction is set with the link parameters as a remorte I/O station.
D9201	LWTP execution result	0 : Normal 2 : LWTP instruction setting fault 3 : Corresponding station error 4 : LWTP cannao be executed in the corresponding station	Stores the execution result of an LWTP (word device write) instruction (M9203 ON). • LWTP instruction setting fault: Faulty setting of the LWTP instruction constant, source, and/or target. • Corresponding station error: The designated station is not executing data link processing. • LWTP instruction cannot be executed by thecorrespopnding station:thestation designated with the LWTP instruction is set with the link parameters as a remorte I/O station.
D9202	Local station link type	Stores the status of station 1 to station 16	Stores whether a slave station is compatible with the MELSECNET mode or MELSECNET II mode. • MELSECNET-compatible station : "0" • MELSECNET II-compatible station : "1"
D9203		Stores the status of station 17 to station 32	
D9241		Stores the status of station 33 to station 48	
D9242		Stores the status of station 49 to station 64	

DEVICE NUMBER	Bit															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
D9202	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1
D9203	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17
D9241	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33
D9242	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49

Device Number	Name	Data	Description
D9204	Link status	0 : Data link in forward loop 1 : Data link in reverse loop 2 : Loopback in forward/ reverse direction 3 : Loopback in forward direction 4 : Loopback in reverse direction 5 : Data link impossible	Stores the current path of the data link. (1) Forward loop  (2) Reverse loop  • Forward/reverse loop  • Forward loopback  • Reverse loopback  • "5" is stored because the watchdog timer setting is too small. • The data in D9204 is updated each time the link status changes.

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9205</td><td>Loopback execution station</td><td>Station executing forward loopback</td><td rowspan="2">• Stores the number of local station or remote I/O station at which loopback is being executed.
 
</td></tr>
<tr><td>D9206</td><td>Loopback execution station</td><td>Station executing reverse loopback</td></tr>
<tr><td>D9207</td><td rowspan="3">Link scan time</td><td>Maximum value</td><td rowspan="3">• Stores the time used for data link processing (link scan time) by all of the local stations and remote I/O stations in the loop currently being used for data link.
• Link scan time definition:
When M > LS
 

When M < LS
 

M : Sequence program scan time by master station
LS : Link scan time (data link processing)</td></tr>
<tr><td>D9208</td><td>Minimum value</td></tr>
<tr><td>D9209</td><td>Current value</td></tr>
<tr><td>D9210</td><td>Retry count</td><td>Total number stored</td><td>• Stores the total number of retries conducted when a transmission error occurs.
• Definition of retry processing:
If data is lost or becomes unreliable due to the occurrence of a data transmission processing error, the same data is sent again.
• Counting stops if the number of retries exceeds the maximum limit "FFFF$_H$".
• Execute reset operation to clear the data to "0".</td></tr>
<tr><td>D9211</td><td>Loop switching count</td><td>Total number stored</td><td>• Stores the total number of times that the forward loop is switched to a reverse loop or to loopback.
• Counting stops if the number of switches exceeds the maximum limit "FFFF$_H$".
• Execute reset operation to clear the data to "0".</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9212</td><td rowspan="4">Local station operation status</td><td>Stores the status of station 1 to station 16</td><td rowspan="4">• Stores the status of all local stations that are in STOP or PAUSE.
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><th></th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9212</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9213</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9214</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9215</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>• When the status of a local station changes to STOP or PAUSE, the corresponding bit is set.
The bit status of remote I/O station always remains "0", indicating RUN.
Example:
When the operation status of station 7 changes to the STOP, "1" is set to bit 6 of D9212. When D9212 is monitored, its value is "64 (40H)".</td></tr>
<tr><td>D9213</td><td>Stores the status of station 17 to station 32</td></tr>
<tr><td>D9214</td><td>Stores the status of station 33 to station 48</td></tr>
<tr><td>D9215</td><td>Stores the status of station 49 to station 64</td></tr>
<tr><td>D9216</td><td rowspan="4">Local station error detection</td><td>Stores the status of station 1 to station 16</td><td rowspan="4">• Stores the numbers of the station that detect the occurrence of an error at another station.
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><th></th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9216</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9217</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9218</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9219</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>• When a normally operating local station detects an error at another local station, the bit corresponding to the normally operating station is set. The bit status of remote I/O station always remains "0".
Example:
When station 5 detects that station 4 is faulty, "1" is set to bit 4 of D9216. When D9216 is monitored, its value is "16 (10H)".
• When the faulty station recovers normal operating status or when the loop line is switched so that the data link returns to normal operating status, the bit is automatically reset to "0".</td></tr>
<tr><td>D9217</td><td>Stores the status of station 17 to station 32</td></tr>
<tr><td>D9218</td><td>Stores the status of station 33 to station 48</td></tr>
<tr><td>D9219</td><td>Stores the status of station 49 to station 64</td></tr>
<tr><td>D9220</td><td rowspan="4">Local station parameter mismatched or remote I/O station input/output allocation error</td><td>Stores the status of station 1 to station 16</td><td rowspan="4">• Stores the numbers of the stations at which a link parameter error sent from the master station is detected by another local or remote I/O station.
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><th></th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9220</td><td>L/R 16</td><td>L/R 15</td><td>L/R 14</td><td>L/R 13</td><td>L/R 12</td><td>L/R 11</td><td>L/R 10</td><td>L/R 9</td><td>L/R 8</td><td>L/R 7</td><td>L/R 6</td><td>L/R 5</td><td>L/R 4</td><td>L/R 3</td><td>L/R 2</td><td>L/R 1</td></tr><tr><td>D9221</td><td>L/R 32</td><td>L/R 31</td><td>L/R 30</td><td>L/R 29</td><td>L/R 28</td><td>L/R 27</td><td>L/R 26</td><td>L/R 25</td><td>L/R 24</td><td>L/R 23</td><td>L/R 22</td><td>L/R 21</td><td>L/R 20</td><td>L/R 19</td><td>L/R 18</td><td>L/R 17</td></tr><tr><td>D9222</td><td>L/R 48</td><td>L/R 47</td><td>L/R 46</td><td>L/R 45</td><td>L/R 44</td><td>L/R 43</td><td>L/R 42</td><td>L/R 41</td><td>L/R 40</td><td>L/R 39</td><td>L/R 38</td><td>L/R 37</td><td>L/R 36</td><td>L/R 35</td><td>L/R 34</td><td>L/R 33</td></tr><tr><td>D9223</td><td>L/R 64</td><td>L/R 63</td><td>L/R 62</td><td>L/R 61</td><td>L/R 60</td><td>L/R 59</td><td>L/R 58</td><td>L/R 57</td><td>L/R 56</td><td>L/R 55</td><td>L/R 54</td><td>L/R 53</td><td>L/R 52</td><td>L/R 51</td><td>L/R 50</td><td>L/R 49</td></tr></table>Example:
When station 5 (local station) is set as a remote I/O station, "1" is set for bit 4 of D9220. When D9220 is monitored, its value is "16 (10H)".
• When the link parameter settings is corrected and the status of the master station is switched from STOP to RUN, the bit is automatically reset to "0".</td></tr>
<tr><td>D9221</td><td>Stores the status of station 17 to station 32</td></tr>
<tr><td>D9222</td><td>Stores the status of station 33 to station 48</td></tr>
<tr><td>D9223</td><td>Stores the status of station 49 to station 64</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9224</td><td rowspan="4">Initial communication between local and/or remote I/O stations</td><td>Stores the status of station 1 to station 16</td><td rowspan="4">• Stores the number of the local or remote I/O stations communicating initial data (link parameters)

DEVICE NUMBER | Bit
b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
D9224: L/R 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
D9225: L/R 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
D9226: L/R 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
D9227: L/R 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49

• When a local station or a remote I/O station is communicating initial setting data (link parameters), the bit corresponding to the station numberm is set.
Example:
When station 23 and station 45 are communicating initial setting data (link parameters), "1" is set to bit 6 of D9225 and bit 12 of D9226. When D9225 is monitored, its value is "64 (40H)" and when D9226 is monitored, its value is "4096 (1000H)".
• When the communication of initial setting data is complete, the bit is automatically reset to "0".</td></tr>
<tr><td>D9225</td><td>Stores the status of station 17 to station 32</td></tr>
<tr><td>D9226</td><td>Stores the status of station 33 to station 48</td></tr>
<tr><td>D9227</td><td>Stores the status of station 49 to station 64</td></tr>
<tr><td>D9228</td><td rowspan="4">Local station or remote I/O station error</td><td>Stores the status of station 1 to station 16</td><td rowspan="4">• Stores the number of the station (local station or remote I/O station) in the data link that is determined by the master station to be faulty.

• A station is determined to be faulty if the data returned from it to the master station is not received within the specified length of time.

DEVICE NUMBER | Bit
b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
D9228: L/R 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
D9229: L/R 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
D9230: L/R 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
D9231: L/R 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49

• When data is not received within the specified length of time, the bit corresponding to the station number of the local station is set.
Example:
When an error at station 3 causes it to fail to return the data to the master station, "1" is set for bit 2 of D9228. When D9228 is monitored, its value is "4".
• When the loop line becomes faulty, "1" is set for the bits if the stations downstream the faulty point or for all local stations.
• When the master station becomes faulty or the setting for the watchdog timer is too small, "1" is set for the bits corresponding to all local stations.
• When the faulty station recovers normal operating status or when the loop line is switched so that the data link returns to normal operating status, the bit is automatically reset to "0".</td></tr>
<tr><td>D9229</td><td>Stores the status of station 17 to station 32</td></tr>
<tr><td>D9230</td><td>Stores the status of station 33 to station 48</td></tr>
<tr><td>D9231</td><td>Stores the status of station 49 to station 64</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9232</td><td rowspan="8">Local station or remote I/O station loop error</td><td>Stores the status of station 1 to station 8</td><td rowspan="8">
• Stores the station number of the local and remote I/O stations at which an error is detected in the forward loop line or reverse loop line.
<table>
<tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr>
<tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td rowspan="2">D9232</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 8</td><td colspan="2">L/R 7</td><td colspan="2">L/R 6</td><td colspan="2">L/R 5</td><td colspan="2">L/R 4</td><td colspan="2">L/R 3</td><td colspan="2">L/R 2</td><td colspan="2">L/R 1</td></tr>
<tr><td rowspan="2">D9233</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 16</td><td colspan="2">L/R 15</td><td colspan="2">L/R 14</td><td colspan="2">L/R 13</td><td colspan="2">L/R 12</td><td colspan="2">L/R 11</td><td colspan="2">L/R 10</td><td colspan="2">L/R 9</td></tr>
<tr><td rowspan="2">D9234</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 24</td><td colspan="2">L/R 23</td><td colspan="2">L/R 22</td><td colspan="2">L/R 21</td><td colspan="2">L/R 20</td><td colspan="2">L/R 19</td><td colspan="2">L/R 18</td><td colspan="2">L/R 17</td></tr>
<tr><td rowspan="2">D9235</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 32</td><td colspan="2">L/R 31</td><td colspan="2">L/R 30</td><td colspan="2">L/R 29</td><td colspan="2">L/R 28</td><td colspan="2">L/R 27</td><td colspan="2">L/R 26</td><td colspan="2">L/R 25</td></tr>
<tr><td rowspan="2">D9236</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 40</td><td colspan="2">L/R 39</td><td colspan="2">L/R 38</td><td colspan="2">L/R 37</td><td colspan="2">L/R 36</td><td colspan="2">L/R 35</td><td colspan="2">L/R 34</td><td colspan="2">L/R 33</td></tr>
<tr><td rowspan="2">D9237</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 48</td><td colspan="2">L/R 47</td><td colspan="2">L/R 46</td><td colspan="2">L/R 45</td><td colspan="2">L/R 44</td><td colspan="2">L/R 43</td><td colspan="2">L/R 42</td><td colspan="2">L/R 41</td></tr>
<tr><td rowspan="2">D9238</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 56</td><td colspan="2">L/R 55</td><td colspan="2">L/R 54</td><td colspan="2">L/R 53</td><td colspan="2">L/R 52</td><td colspan="2">L/R 51</td><td colspan="2">L/R 50</td><td colspan="2">L/R 49</td></tr>
<tr><td rowspan="2">D9239</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr>
<tr><td colspan="2">L/R 64</td><td colspan="2">L/R 63</td><td colspan="2">L/R 62</td><td colspan="2">L/R 61</td><td colspan="2">L/R 60</td><td colspan="2">L/R 59</td><td colspan="2">L/R 58</td><td colspan="2">L/R 57</td></tr>
</table>
F: Forward loop line
R: Reverse loop line
• When an error is detected at a local station and/or remote I/O station in the forward loop line or the reverse loop line, the corresponding bit is set.
Example:
When an error is detected in the forward loop line at station 5, "1" is set for bit 8 of D9232. When D9232 is monitored, its value is "256 (100H)".
This error will have been caused by one of the following:
(a) A faulty connection of the forward loop cable connecting station 4 and station 5
(b) A fault of the forward loop receive end of data link module in station 5
(c) A fault of the forward loop send end of data link module in station 4
• With errors other than loop line errors, such as hardware errors and data communication errors, only the error involved with the loop line currently being used will be detected. The error status is retained.
• When data link is executed again with the loop line in which an error was detected, the bit data is automatically reset to "0" provided that the fault has been removed.
</td></tr>
<tr><td>D9233</td><td>Stores the status of station 9 to station 16</td></tr>
<tr><td>D9234</td><td>Stores the status of station 17 to station 24</td></tr>
<tr><td>D9235</td><td>Stores the status of station 25 to station 32</td></tr>
<tr><td>D9236</td><td>Stores the status of station 33 to station 40</td></tr>
<tr><td>D9237</td><td>Stores the status of station 41 to station 48</td></tr>
<tr><td>D9238</td><td>Stores the status of station 49 to station 56</td></tr>
<tr><td>D9239</td><td>Stores the status of station 57 to station 64</td></tr>
<tr><td>D9240</td><td>Receive error detection count</td><td>Stores the total number of receive error occurrences</td><td>
• Stores the number of times that the following errors are detected in the loop line currently being used:
CRC, AB.IF, OVER
• Counting stops if the number of receive error occurrences exceeds the maximum limit "FFFF$_H$".
• Execute the reset operation to clear the data to "0".
</td></tr>
</table>

2) Special link registers effective only for local stations

Device Number	Name	Data	Description
D9243	Station number data of the station itself	Stores a station number (0 to 64)	• Stores the station number assigned to the local station itself. • Used by a local station to check its own station number.
D9244	Slave station number data	Stores a slave station number	• Used by a local station to check the total number of slave stations in the loop.
D9245	Receive error detection count	Stores the total number of receive error occurrences	• Stores the number of times that the following errors are detected in the loop line currently being used: CRC, AB.IF, OVER • Counting stops if the number of receive error occurrences exceeds the maximum limit "FFFFH". • Execute the reset operation to clear the data to "0".
D9248	Local station operating status	Stores the status of station 1 to station 16	• Stores the number of the local stations, excluding the station itself, whose status is either STOP or PAUSE.
D9249		Stores the status of station 17 to station 32	
D9250		Stores the status of station 33 to station 48	
D9251		Stores the status of station 49 to station 64	
D9252	Local station error status	Stores the status of station 1 to station 16	• Stores the number of the local station in the loop at which a fault is detected. • Only a faulty local station can be detected by another local station. The bit status of remote I/O station always remains "0".
D9253		Stores the status of station 17 to station 32	
D9254		Stores the status of station 33 to station 48	
D9255		Stores the status of station 49 to station 64	

DEVICE NUMBER	Bit															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
D9248	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1
D9249	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17
D9250	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33
D9251	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49

• When the status of a local station is either STOP or PAUSE, the corresponding bits are set. When the status of the local station changes to RUN or STEP RUN, the bit is automatically reset to "0". The bit status of remote I/O station always remains "0".

Example:
"When the statuses of local station 7 and local station 15 are either STOP or PAUSE, "1" is set to bit 6 and bit 14 of D9248. When D9248 is monitored, its value is "16448 (4040H)".

• The bit corresponding to the station itself is not set regardless of the status of the station itself.

DEVICE NUMBER	Bit															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
D9252	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1
D9253	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17
D9254	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33
D9255	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49

• Only a faulty local station can be detected by another local station. The bit status of remote I/O station always remains "0".

• When a fault is detected at a local station (other than the station itself) the corresponding bit is set.

Example:
When local station 12 is faulty, "1" is set to bit 11 of D9252. When D9252 is monitored, its value is "2048 (500H)".

• When the faulty station recovers normal operating status or when the loop line is switched so that the data link returns to normal operating status, the bit is automatically reset to "0".

5.5.2 MELSECNET/B data link

(1) Special link relays

1) Special link relays effective only for the master station

Device Number	Name	Data	Description
M9200	LRDP instruction received	OFF : Unreceived ON : Received	• Turned ON when an LRDP (word device read) instruction is received. • Used in a user program as an interlock for an LRDP instruction. • Remains ON after the completion of word device read processing called by an LRDP instruction. Turned OFF with an RST instruction in a user program.
M9201	LRDP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON after an LRDP (word device read) instruction has been executed. The execution results are stored in D9200. • Used as a conditional contact to reset M9200 and M9201 after the completion of word device read processing called by an LRDP instruction. • Turned OFF with an RST instruction in a user program after it has been turned ON.
M9202	LWTP instruction received	OFF : Unreceived ON : Received	• Turned ON when an LWTP (word device write) instruction is received. • Used in a user program as an interlock for an LWTP instruction. • Remains ON after the completion of word device write processing called by an LWTP instruction. Turned OFF with an RST instruction in a user program.
M9203	LWTP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON after an LWTP (word device write) instruction has been executed. The execution results are stored in D9201. • Used as a conditional contact to reset M9202 and M9203 after the completion of word device write processing called by an LWTP instruction. • Turned OFF with an RST instruction in a user program.
M9206	Link parameter error in the station itself	OFF : Normal ON : Error	• Turned ON when link parameter of the station itself is not set or the setting is incorrect. • Turned OFF with an RST instruction in a user program.
M9207	Link parameter check result	OFF : Normal ON : Error	• Goes ON if a lower tier link uses device ranges (B, W) outside the range set by a master station, in the upper tier link, for itself. • Check is executed only when M9209 is ON.
M9208	B and W transmission range for the master station (lower tier master stations only)	OFF : To the second and third tiers ON : To the second tier only	• Sets whether the B and W data controlled by the master station in the upper tier is sent to the local stations (sub-slave stations) in the lower tier.
M9209	Link parameter check instruction (lower tier link master stations only)	OFF : Check executed ON : Check not executed	• To be turned ON when the link devices (B and W) used by the upper tier and the link devices (B and W) used by the lower tier are not compared for "match". • When M9209 is OFF, the link parameters for the upper tier and the link parameters for the lower tier are checked.
M9210	Link card error (master station)	OFF : Normal ON : Error	• Turned ON when the link card hardware is faulty.

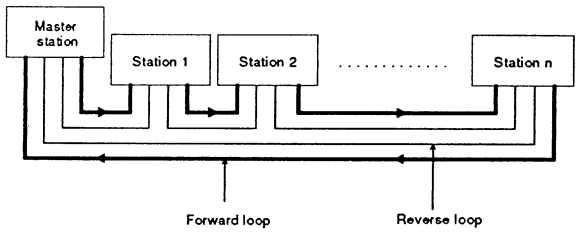
Device Number	Name	Data	Description
M9224	Link status	OFF : Offline ON : Online, station-to-station test, or self-loopback test	• Turned ON when the master station is offline, in the station-to-station test mode, or in the self-loopback test mode. • Turned OFF when the master station is reset after being placed in the online mode.
M9232	Local station operating status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of the local station. • Turned ON when the status of any local station in the loop changes to STOP or PAUSE. • Turned OFF automatically when the status of all local stations changes to RUN or STEP RUN. That is, M9232 is turned OFF when bits D9212 to D9215 are all OFF.
M9233	Local station error detected	OFF : No error ON : Error detected	• Turned ON when a local station in the executed loop detects an error in another station (M9255 ON). • Automatically turned OFF when the faulty station is returned to the normal state or the data link returns to the normal status by switching the loop line. That is, M9233 is turned OFF when bits D9216 to D9219 are all OFF.
M9235	Local station parameter error detected	OFF : No error ON : Error detected	• Turned ON when the bit device range (link relays and link registers) outside the range allocated to a master station for the lower tier is allocated with the link parameters for the lower tier. • Turned OFF when the error is eliminated by correcting the link parameters. That is, M9235 is turned OFF when bits D9220 to D9223 are all OFF.
M9236	Local station initial communications status	OFF : Not communicating ON : Communicating	• Turned ON while a local station is communicating the initial setting data (link parameters) to a master station to execute data link processing. • Automatically turned OFF when the communication for initial data setting has been completed. That is, M9236 is turned OFF when bits D9224 to D9227 are all OFF.
M9237	Local station error	OFF : Normal ON : Error	• Turned ON when an error occurs at one local station within the loop. (The relay is turned ON while a station-to-station test is being executed for a local station and the data link is operating.) • Automatically turned OFF when the faulty station returns to normal. That is, M9237 is turned OFF when bits D9228 and D9229 are all OFF.

2) Special link relays effective only for local stations

Device Number	Name	Data	Description
M9204	LRDP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON by a local station upon the completion of word device read processing called by an LRDP instruction.
M9205	LWTP instruction completed	OFF : Uncompleted ON : Completed	• Turned ON by a local station upon the completion of word device write processing called by an LRDP instruction.
M9211	Link card error (local station)	OFF : Normal ON : Error	• Turned ON when the link card hardware is faulty.
M9240	Link status	OFF : Online ON : Offline, station-to-station test, or self-loopback test	• Turned ON when the station itself is offline, in the station-to-station test mode, or in the self-loopback test mode. • Turned OFF when the station itself is reset after being placed in the online mode.
M9246	Data unreceived	OFF : Received ON : Unreceived	• Turned ON when the data from the master station has not been received.
M9247	Data unreceived	OFF : Received ON : Unreceived	• In the three-tier system, M9247 is turned ON when the data from the master station for the third tier has not been received by a sub-slave station. That is, M9247 is ON while M9208 is ON.
M9250	Parameter unreceived	OFF : Received ON : Unreceived	• Turned ON when the link parameters have not been received from the master station. • Automatically turned OFF when the link parameter is received. • Only effective while the loop line in which the data link is executed is online.
M9251	Link break	OFF : Normal ON : Break	• ON/OFF status depends on whether the station itself stopped the data link. • Automatically turned OFF when the data link returns to the normal status. • Only effective while the loop line in which the data link is executed is online.
M9253	Master station operating status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of a master station. • Turned ON when the status of the master station is either STOP or PAUSE. • Turned OFF when the status of the master station changes to RUN or STEP RUN.
M9254	Operating status of other local stations	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	• ON/OFF status depends on the operation status of a local station other than the station itself. • Turned ON when the status of a local station in the loop (other than the station itself) is either STOP or PAUSE. • Not turned ON when the status of the station itself is either STOP or PAUSE. • Automatically turned OFF when the status of a local station in the loop (other than the station itself) changes to RUN or STEP RUN. That is, M9254 is turned OFF when bits D9248 and D9249 are OFF.
M9255	Error status of other local stations	OFF : Normal ON : Error	• ON/OFF status depends on the operation status of a local station other than the station itself. • Turned ON when an error occurs with one local station in the loop (other than the station itself). • Automatically turned OFF when the faulty station returns to the normal state or the data link returns to the normal state by switching the loop line. That is, M9255 is turned OFF when bits D9252 to D9253 are all OFF.

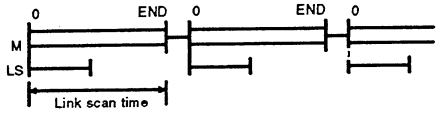
(2) Special link registers

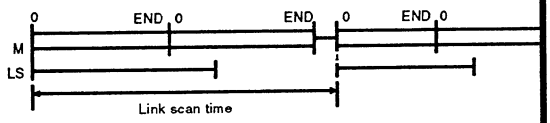
1) Special link registers effective only for the master station

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9200</td><td>LRDP execution result</td><td>0 : Normal
2 : LRDP instruction setting fault
3 : Corresponding station error</td><td>Stores the execution result of an LRDP (word device read) instruction (M9201 ON).
• LRDP instruction setting fault:
Faulty setting of the LRDP instruction constant, source, and/or target.
• Corresponding station error:
The designated station is not executing data link processing.</td></tr>
<tr><td>D9201</td><td>LWTP execution result</td><td>0 : Normal
2 : LWTP instruction setting fault
3 : Corresponding station error</td><td>Stores the execution result of an LWTP (word device write) instruction (M9203 ON).
• LWTP instruction setting fault:
Faulty setting of the LWTP instruction constant, source, and/or target.
• Corresponding station error:
The designated station is not executing data link processing.</td></tr>
<tr><td>D9202</td><td rowspan="2">Local station link type</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">Stores whether a slave station is compatible with the MELSECNET mode or MELSECNET II mode.
• MELSECNET-compatible station : "0"
• MELSECNET II-compatible station : "1"
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9202</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9203</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr></table></td></tr>
<tr><td>D9203</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9204</td><td>Link status</td><td>0 : Data link
5 : Data link impossible</td><td>Stores the current path of the data link.
(1) Forward loop
 

• "5" is stored because the watchdog timer setting is too small.
• The data in D9204 is updated each time the link status changes.</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9212</td><td rowspan="2">Local station operation status</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the status of all local stations that are in STOP or PAUSE.
<table>
<tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr>
<tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td>D9212</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr>
<tr><td>D9213</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr>
</table>
• When the status of a local station changes to STOP or PAUSE, the corresponding bit is set.
Example:
When the operation status of station 7 changes to the STOP, state, 1 is set to bit 6 of D9212. When D9212 is monitored, its value is 64 (40_H).</td></tr>
<tr><td>D9213</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9216</td><td rowspan="2">Local station error detection</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the numbers of the station that detect the occurrence of an error at another station.
<table>
<tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr>
<tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td>D9216</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr>
<tr><td>D9217</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr>
</table>
• When a normally operating local station detects an error at another local station, the bit corresponding to the normally operating station is set. The bit status of remote I/O station always remains "0".
Example:
When station 5 detects that station 4 is faulty, "1" is set to bit 4 of D9216. When D9216 is monitored, its value is "16 (10_H)".
• When the faulty station recovers normal operating status or when the loop line is switched so that the data link returns to normal operating status, the bit is automatically reset to "0".</td></tr>
<tr><td>D9217</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9220</td><td rowspan="2">Local station parameter mismatched or remote I/O station input/output allocation error</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the numbers of the stations at which a link parameter error sent from the master station is detected by another local or remote I/O station.
<table>
<tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr>
<tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr>
<tr><td>D9220</td><td>L/R 16</td><td>L/R 15</td><td>L/R 14</td><td>L/R 13</td><td>L/R 12</td><td>L/R 11</td><td>L/R 10</td><td>L/R 9</td><td>L/R 8</td><td>L/R 7</td><td>L/R 6</td><td>L/R 5</td><td>L/R 4</td><td>L/R 3</td><td>L/R 2</td><td>L/R 1</td></tr>
<tr><td>D9221</td><td>L/R 0</td><td>L/R 31</td><td>L/R 30</td><td>L/R 29</td><td>L/R 28</td><td>L/R 27</td><td>L/R 26</td><td>L/R 25</td><td>L/R 24</td><td>L/R 23</td><td>L/R 22</td><td>L/R 21</td><td>L/R 20</td><td>L/R 19</td><td>L/R 18</td><td>L/R 17</td></tr>
</table>
• When the link parameter settings is corrected and the status of the master station is switched from STOP to RUN, the bit is automatically reset to "0".</td></tr>
<tr><td>D9221</td><td>Stores the status of station 17 to station 31</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9207</td><td rowspan="3">Link scan time</td><td>Maximum value</td><td rowspan="3">• Stores the time used for data link processing (link scan time) by all of the local stations and remote I/O stations in the loop currently being used for data link.
• Link scan time definition:
When M > LS
 

When M < LS
 

M : Sequence program scan time by master station
LS : Link scan time (data link processing)</td></tr>
<tr><td>D9208</td><td>Minimum value</td></tr>
<tr><td>D9209</td><td>Current value</td></tr>
<tr><td>D9210</td><td>Retry count</td><td>Total number stored</td><td>• Stores the total number of retries conducted when a transmission error occurs.
• Definition of retry processing:
If data is lost or becomes unreliable due to the occurrence of a data transmission processing error, the same data is sent again.
• Counting stops if the number of retries exceeds the maximum limit "$FFFF_H$".
• Execute reset operation to clear the data to "0".</td></tr>
</table>

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9224</td><td rowspan="2">Initial communicatio n between local stations</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the number of the local stations communicating initial setting data (link parameters)
<table><tr><td>DEVICE NUMBER</td><td colspan="16">Bit</td></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9224</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9225</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr></table>• When a local station is communicating initial setting data (link parameters), the bit corresponding to the station numberm is set.
Example:
When station 23 is communicating initial setting data (link parameters), 1 is set to bit 6 of D9225.
When D9225 is monitored, its value is 64 (40_H).
• When the initial setting data has been communicated, the bit is automatically reset to "0".</td></tr>
<tr><td>D9225</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9228</td><td rowspan="2">Local station error</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the number of the local station in the data link that is determined by a master station to be faulty.
• A station is determined to be faulty if the data returned from it to the master station is not received within the specified length of time.
<table><tr><td>DEVICE NUMBER</td><td colspan="16">Bit</td></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9228</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9229</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr></table>• When data is not received within the specified length of time, the bit corresponding to the station number of the local station is set.
Example:
When an error at station 3 causes it to fail to return the data to the master station, "1" is set for bit 2 of D9228.
When D9228 is monitored, its value is "4".
• When the loop line becomes faulty, "1" is set for the bits of the stations after the fault or for all local stations.
• When the master station becomes faulty or the setting for the watchdog timer is too small, "1" is set for the bits corresponding to all local stations.
• When a master station becomes fauly or the setting for the watching timer is too small, 1 is set for the bits corresponding to all local stations.
• when the faulty station returns to nomal, the bit is automatically reset to "0".</td></tr>
<tr><td>D9229</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9240</td><td>Receive error detection count</td><td>Stores the total number of receive errors</td><td>• Stores the number of times that the following errors are detected in the loop line currently being used:
CRC, AB.IF, OVER
• Counting stops if the number of receive error occurrences exceeds the maximum limit "$FFFF_H$".
• Execute the reset operation to clear the data to "0".</td></tr>
</table>

2) Special link registers effective only for local stations

<table>
<tr><th>Device Number</th><th>Name</th><th>Data</th><th>Description</th></tr>
<tr><td>D9243</td><td>Station number data of the station itself</td><td>Stores a station number (0 to 64)</td><td>• Stores the station number assigned to the local station itself.
• Used by a local station to check its own station number.</td></tr>
<tr><td>D9244</td><td>Slave station number data</td><td>Stores a slave station number</td><td>• Used by a local station to check the total number of slave stations in the loop.</td></tr>
<tr><td>D9245</td><td>Receive error detection count</td><td>Stores the total number of receive errors</td><td>• Stores the number of times that the following errors are detected in the loop line currently being used:
CRC, AB.IF, OVER
• Counting stops if the number of receive error occurrences exceeds the maximum limit "FFFFH".
• Execute the reset operation to clear the data to "0".</td></tr>
<tr><td>D9248</td><td rowspan="2">Local station operating status</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the number of the local stations, excluding the station itself, whose status is either STOP or PAUSE.
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9248</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9249</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr></table>• When the status of a local station is either STOP or PAUSE, the corresponding bits are set. When the status of the local station changes to RUN or STEP RUN, the bit is automatically reset to "0". The bit status of remote I/O station always remains "0".
Example:
"When the statuses of local station 7 and local station 15 are either STOP or PAUSE, "1" is set to bit 6 and bit 14 of D9248. When D9248 is monitored, its value is "16448 (4040H)".
• The bit corresponding to the station itself is not set regardless of the status of the station itself.</td></tr>
<tr><td>D9249</td><td>Stores the status of station 17 to station 31</td></tr>
<tr><td>D9252</td><td rowspan="2">Local station error status</td><td>Stores the status of station 1 to station 16</td><td rowspan="2">• Stores the number of the local station in the loop at which a fault is detected.
• Only a faulty local station can be detected by another local station. The bit status of remote I/O station always remains "0".
<table><tr><th>DEVICE NUMBER</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9252</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9253</td><td>0</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr></table>• When a fault is detected at a local station (other than the station itself) the corresponding bit is set.
Example:
When local station 12 is faulty, "1" is set to bit 11 of D9252. When D9252 is monitored, its value is "2048 (500H)".
• When the faulty station recovers normal operating status or when the loop line is switched so that the data link returns to normal operating status, the bit is automatically reset to "0".</td></tr>
<tr><td>D9253</td><td>Stores the status of station 17 to station 31</td></tr>
</table>

5.6 Self-Diagnosis Function

The self-diagnosis function checks the data link module hardware and the fiber-optic cables and coaxial cables for breakage.

The following is checked by the self-diagnosis function:

Check Item	Description	MELSEC-NET	MELSEC-NET/B
Forward loop test	Every fiber-optic cable or coaxial cable in the data link system is checked. The forward loop, in which the data link is established during normal operation, is also checked.	O	-
Reverse loop test	Every fiber-optic cable or coaxial cable in the data link system is checked. The reverse loop, in which the data link is established when an error occurs, is also checked.	O	-
Station-to-station test (master station)	The fiber-optic cables or coaxial cables connecting the two stations are checked. For this check, the station with the lower station number is designated as the master station and the station with the higher number is designated as the slave station.	O	O
Station-to-station test (slave station)		O	O
Self-loopback test	The hardware of each individual link module, including the transmission and receive circuits, is checked.	O	O

5.6.1 Self-loopback test

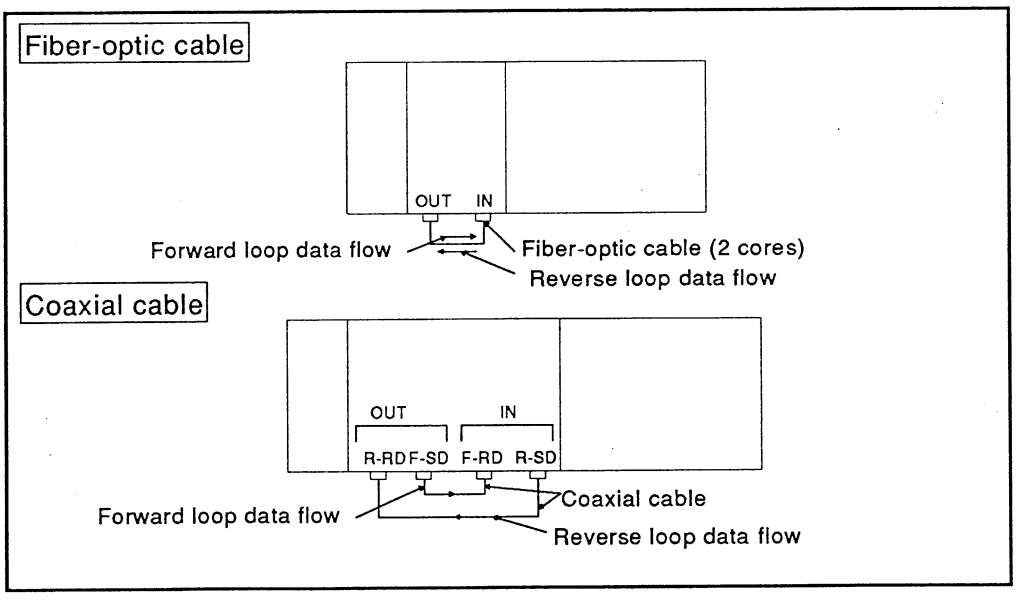
(1) Self-loopback test

(a) The self-loopback test checks the hardware of each individual link module, including the transmission and receive circuits (forward loop and reverse loop).

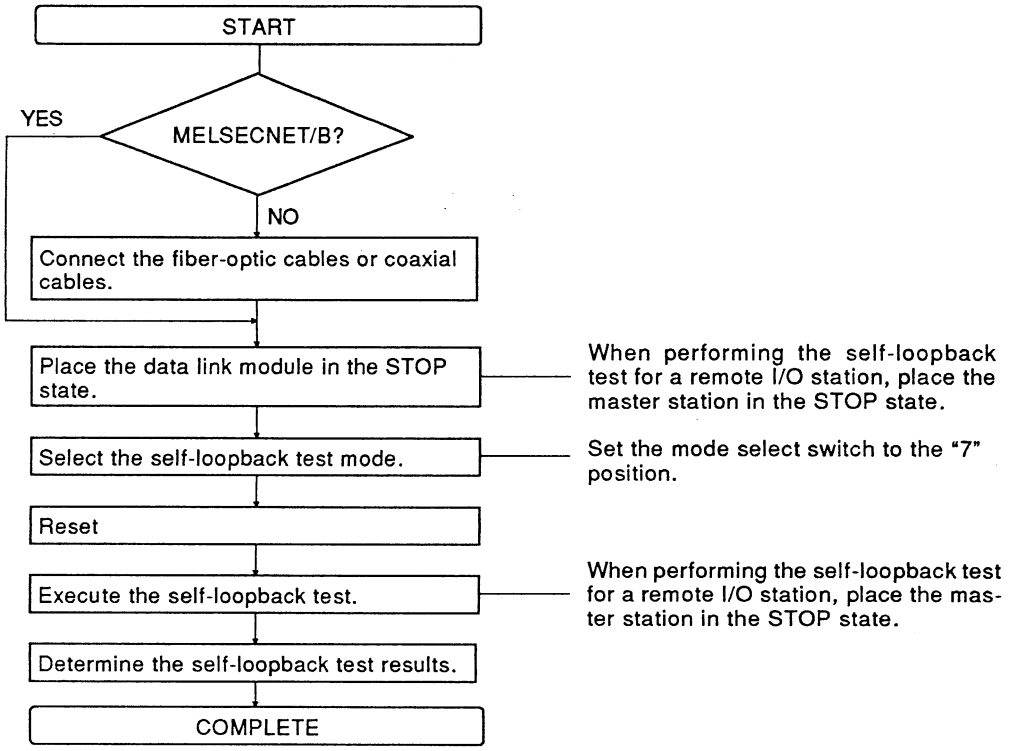
1) In the MELSECNET Data Link System, connect the send and receive ports of the self with a fiber-optic or coaxial cable, as shown in Fig. 8.16.

2) In the MELSECNET/B Data Link System, perform this test with a single link module.

(b) If the data sent from the send end of the forward/reverse loop cannot be received at the receive end within the specified period, the loop is determined to be faulty.



(2) Test sequence



(3) Test results

The test results are indicated by the LED indicators.

(a) Normal

If the test results are normal, the following LED indicators flash in order:
CRC, OVER, AB.IF, TIME, DATA, UNDER

(b) Error

If an error is found, the corresponding LED indicator lights and the test is discontinued.

1) When the F.LOOP, R.LOOP, and TIME LED indicators are lit:
   i) The forward loop cable is broken.
   ii) The forward loop send end and receive end are not connected.
   iii) The forward loop send end is connected to the reverse loop send end and the reverse loop receive end is connected to the forward loop receive end.

(c) When the F.LOOP, R.LOOP, and DATA LED indicators are lit:

1) The reverse loop cable is broken.
2) The reverse loop send end and receive end are not connected.

(d) When an ERROR LED other than those stated above is lit:

1) The hardware is faulty.
2) A cable was disconnected during the test.
3) A cable was broken during the test.

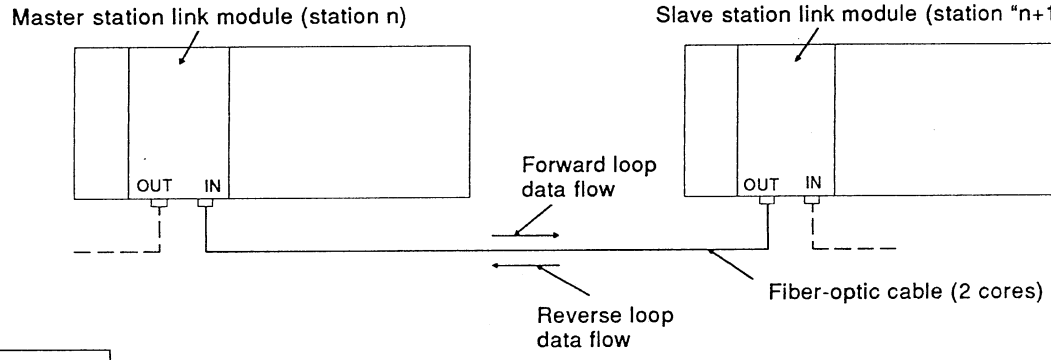
5.6.2 Station-to-station test

(1) Station-to-station test

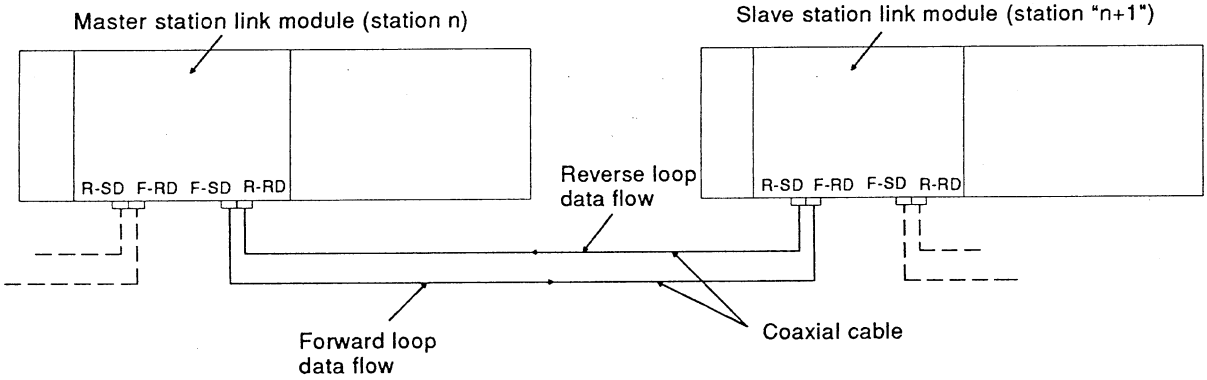
The station-to-station test checks the cable connections of two adjacent stations.

If the data sent from the master station link module is not returned from the slave station link module within the specified period, the loop is determined to be faulty.

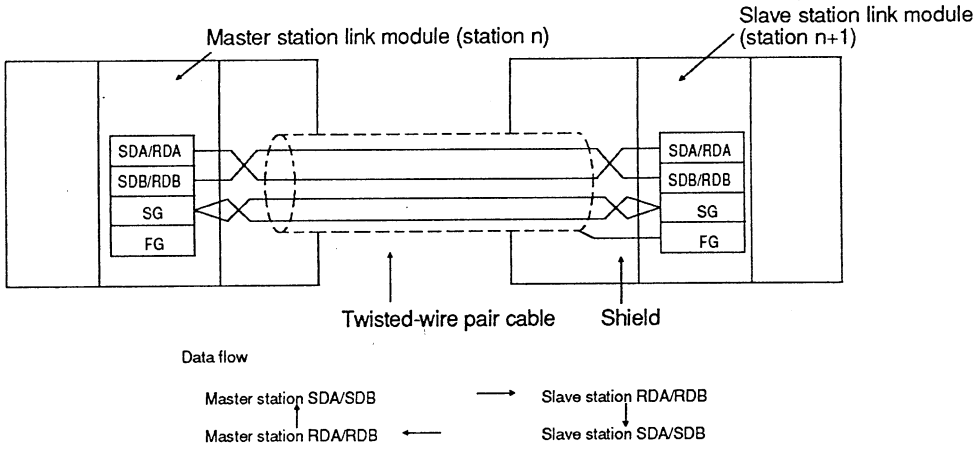
Fiber-optic cable



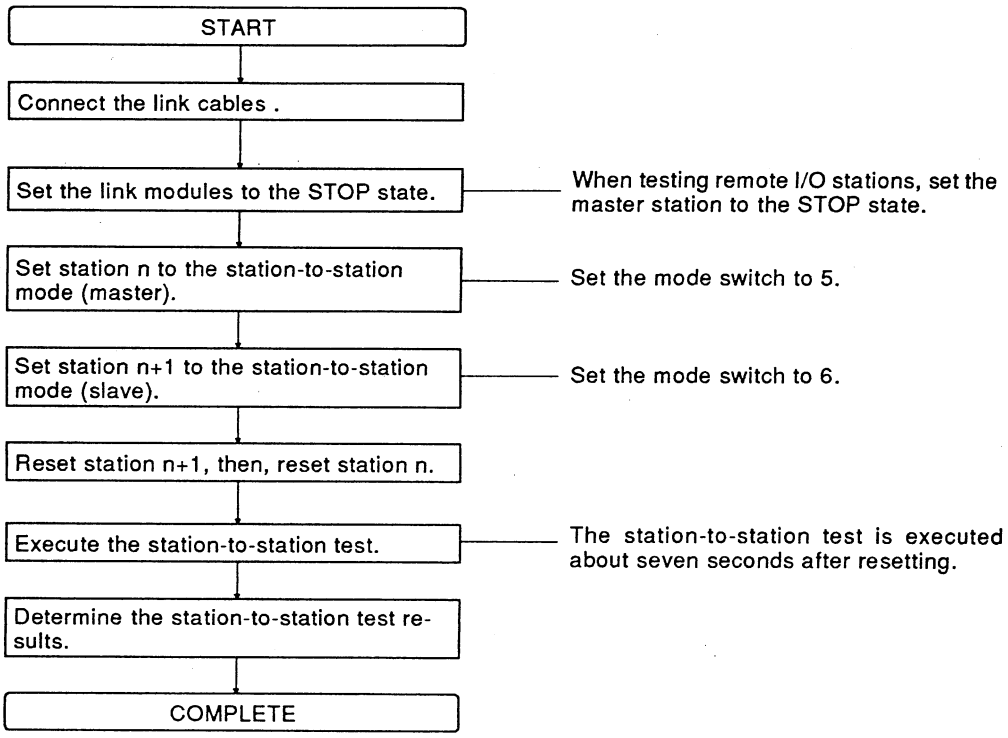
Coaxial cable



When a MELSECNET/B Data Link System is used



(2) Test sequence



(3) Test results

The test results are indicated by the LED indicators.

(a) Normal

If the test results are normal, the following LED indicators flash in order:
CRC, OVER, AB.IF, TIME, DATA, UNDER

(b) Error

If an error is found, the corresponding LED indicator lights and the test is discontinued.

1) When the F.LOOP, R.LOOP, and TIME LED indicators are lit:
   i) The forward loop cable is broken.
   ii) The forward loop send end and receive end are not connected.
   iii) The forward loop send end is connected to the reverse loop send end and the reverse loop receive end is connected to the forward loop receive end.

2) When the F.LOOP, R.LOOP, and DATA LED indicators are lit:
   i) The reverse loop cable is broken.
   ii) The reverse loop send end and receive end are not connected.

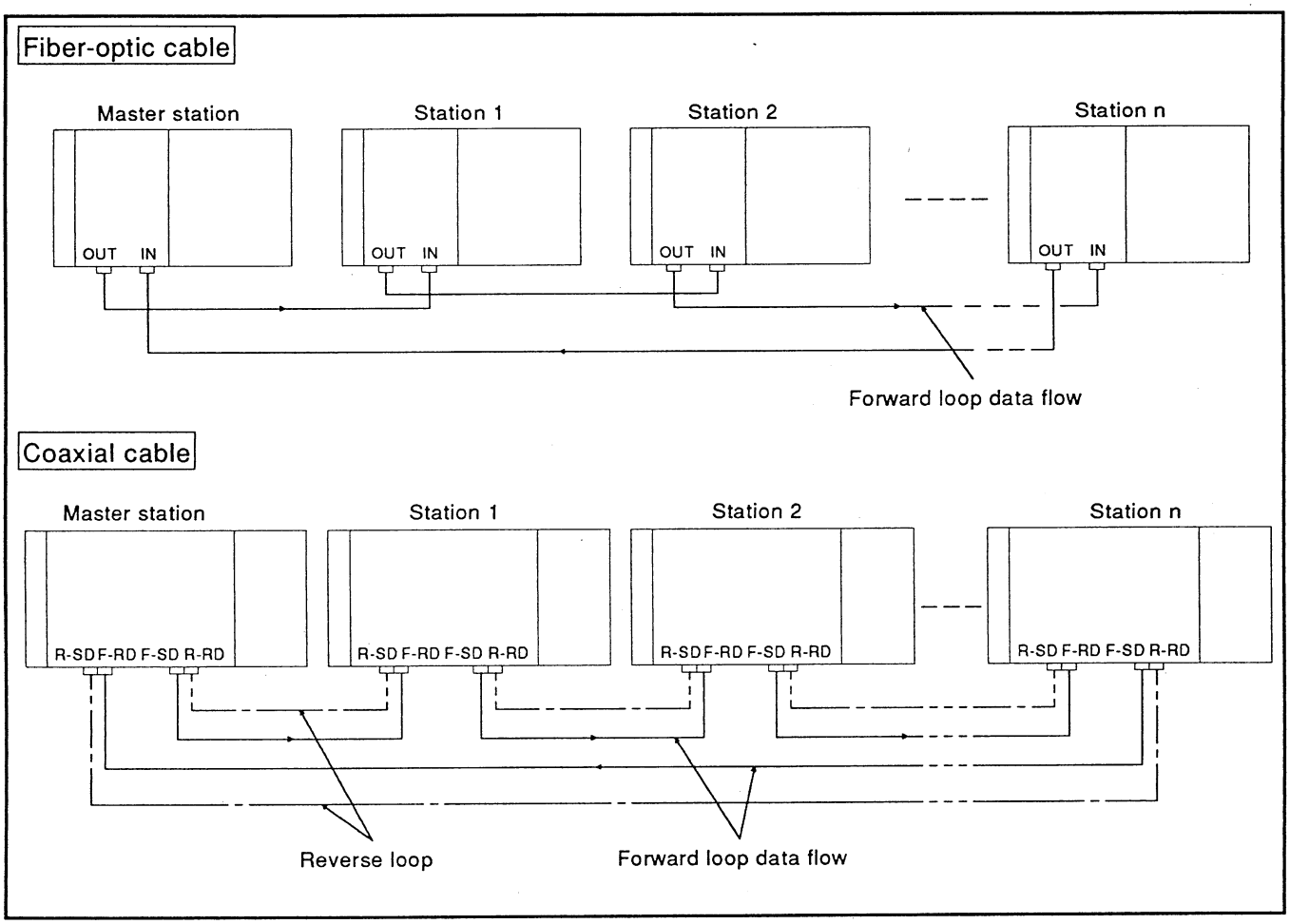
3) When an ERROR LED other than those stated above is lit:
   i) The hardware is faulty.
   ii) A cable was disconnected during the test.
   iii) A cable was broken during the test.

5.6.3 Forward loop test and reverse loop test

(1) Forward loop test

(a) The forward loop test checks the forward loop after the stations are connected with fiber-optic cable or coaxial cable.

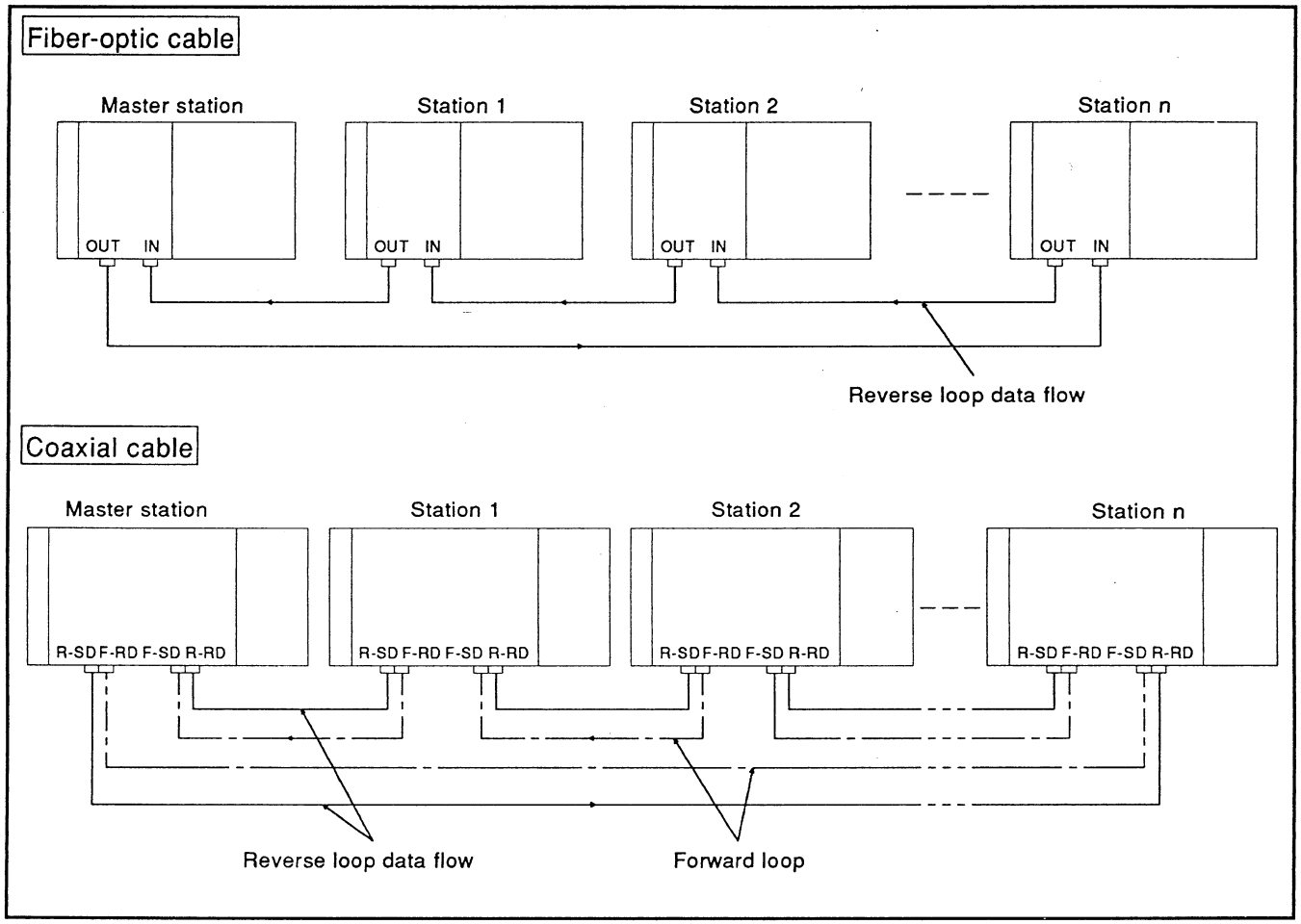
(b) If the data sent from the send end of the master station in the forward loop cannot be received in the forward loop at the receive end of the master station within the specified period, the loop is determined to be faulty.



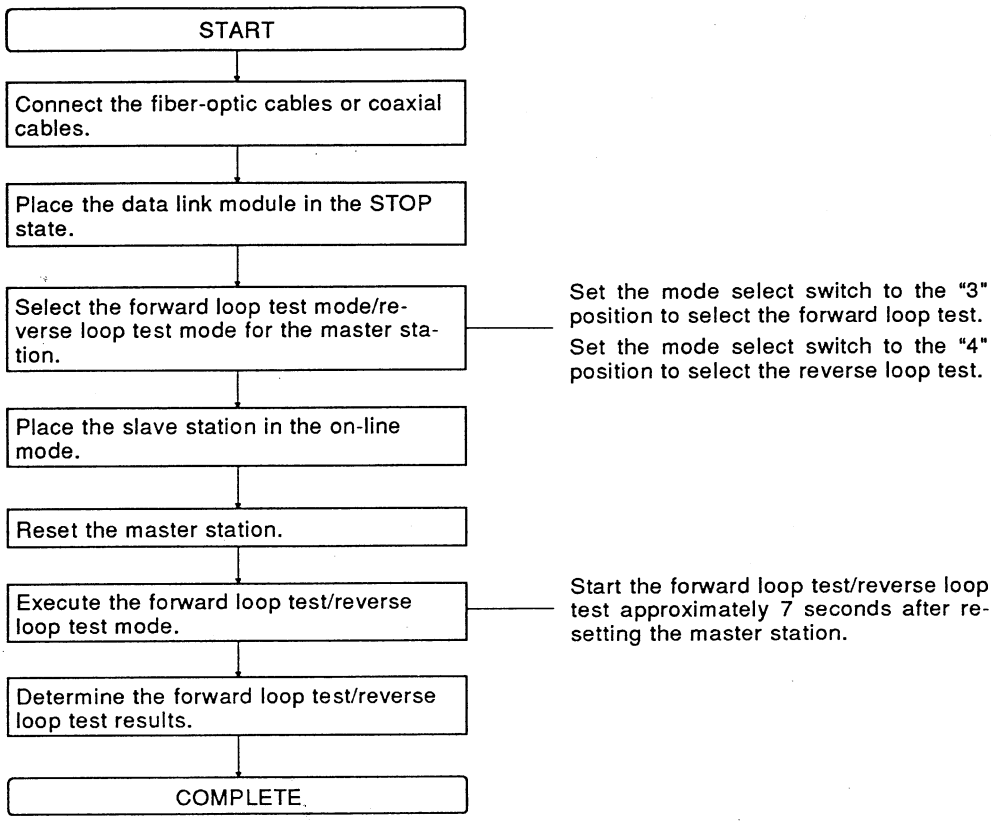
(2) Reverse loop test

(a) The reverse loop test checks the reverse loop after the stations are connected with fiber-optic cable or coaxial cable.

(b) If the data sent from the send end of the master station in the reverse loop cannot be received in the reverse loop at the receive end of the master station within the specified period, the loop is determined to be faulty.



(3) Test sequence



(4) Test results

The test results are indicated by the LED indicators on the data link module or by the link monitor function of the GPP.

(a) Refer to Section 8.1 for details on the link monitor function of the GPP.

(b) The following describes the LED indicators.

1) Normal

If the test results are normal, the following LED indicators flash in order:

CRC, OVER, AB.IF, TIME, DATA, UNDER

2) Error

If an error is found, the corresponding LED indicator lights and the test is discontinued.

i) When the TIME and DATA LED indicators are lit:

- The setting for the watchdog timer is too short.

ii) When the TIME, DATA, and UNDER LED indicators are lit:

- Either the fiber-optic cable/coaxial cable is broken or a slave station is faulty.
- The master station (00) setting is made for more than one station.

POINT

If forward/reverse loop is faulty, the data link will be established in the reverse/forward loop or the loopback mode.

The forward/reverse loop data link will be recovered when the cause of the error is eliminated. The LED indicator will remain in the error state (lit) even after the forward/reverse loop data link is recovered. Reset the master station and execute the forward loop test and the reverse loop test before starting system operation.

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100-8310 TELEX : J24532 CABLE MELCO TOKYO
NAGOYA WORKS : 1-14 , YADA-MINAMI 5 , HIGASHI-KU, NAGOYA , JAPAN

IB(NA)66413-A(9303)MEE